COMPAL CONFIDENTIAL

MODEL NAME : *QALA1*

PCB NO : *LA-7762A (DAZ0LI00100)*

BOM P/N : *4519EJ31L01,4519EJ31L02,4519EJ31L03,4519EJ31L04.*

GPIO P/N: *E4 VC GPIO map rev 1.1*

Dalmore 15 DSC

Ivy Bridge + Panther POINT

2012-02-22

REV : 1.0 (A00)

@ : Nopop Component

CONN@ : Connector Component

MB Type	BOM P/N	
TPM	4319EJ31L01(R3) 4319EJ31L03(R1)	1@ 3@ PS8171@
DTP	4319EJ31L02(R3) 4319EI31L04(R1)	2@ 3@ PS8171@

MB PCB

Part Number	Description
DA80000P600	PCB 0LI LA-7762P REV0 M/B DSC

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Title: Cover Sheet

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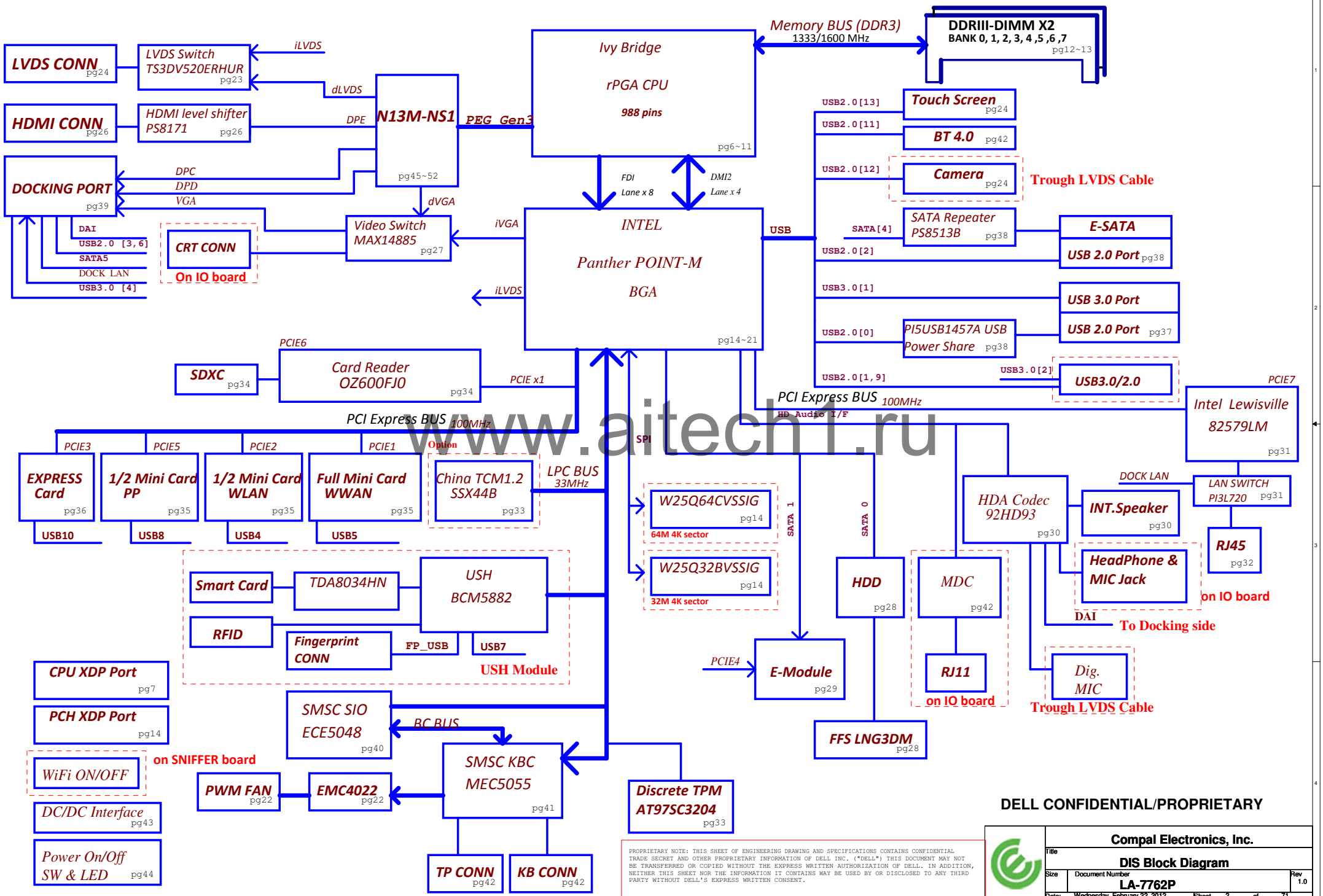
Block Diagram Compal confidential



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Compal Electronics, Inc.		
Title: DIS Block Diagram		
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POWER STATES

Signal / State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane / State	+PWR_SRC +PWR_SRC_S +5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN +GPU_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.50
			Add Plating		1.30
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080	2.60
2	GND1		Copper foil	1.0 oz	1.35
		3.7	Core	4mil	3.91
3	Sig 1		Copper foil	1.0 oz	1.35
		4.3	Prepreg	1506+7628H	13.18
4	GND/PWR		Copper foil	1.0 oz	1.35
		3.7	Core	4mil	3.91
5	Sig2		Copper foil	1.0 oz	1.35
		4.3	Prepreg	1506+7628H	12.48
6	Sig3		Copper foil	1.0 oz	1.35
		3.7	Core	4mil	3.91
7	GND2		Copper foil	1.0 oz	1.35
		3.7	Prepreg	1080	2.60
8	Bottom		Copper foil	0.5oz	0.65
			Add Plating		1.30
			SolderMask		0.50
Overall Thickness (1.4mm ± 10%)		55.1			55.59000
					1.411986

Reference GCE RD data

USB 3.0 PORT#	Connetion
1	JUSB1 (Right side)
2	JUSB2 (Left side)
3	NA
4	DOCKING

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

DSC DP/HDMI Port	Connetion
Port C	Dock DP port 2
Port D	Dock DP port 1
Port E	MB HDMI Conn

	USB PORT#	DESTINATION
PCH	0	JUSB1 (Right side)
	1	JUSB2 (Left side)
	2	JESA1 (Right side ESATA)
	3	DOCKING
	4	WLAN/WIMAX
	5	WWAN/UWB
	6	DOCKING
	7	USH->BIO
	8	JMINI3(Flash)
	9	JUSB (Left side)
	10	Express card
	11	Bluetooth
	12	Camera
	13	LCD Touch

USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	1/2 MINI CARD-3 PCIE
Lane 6	Card Reader
Lane 7	10/100/1G LOM
Lane 8	None

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Title: Index and Config.

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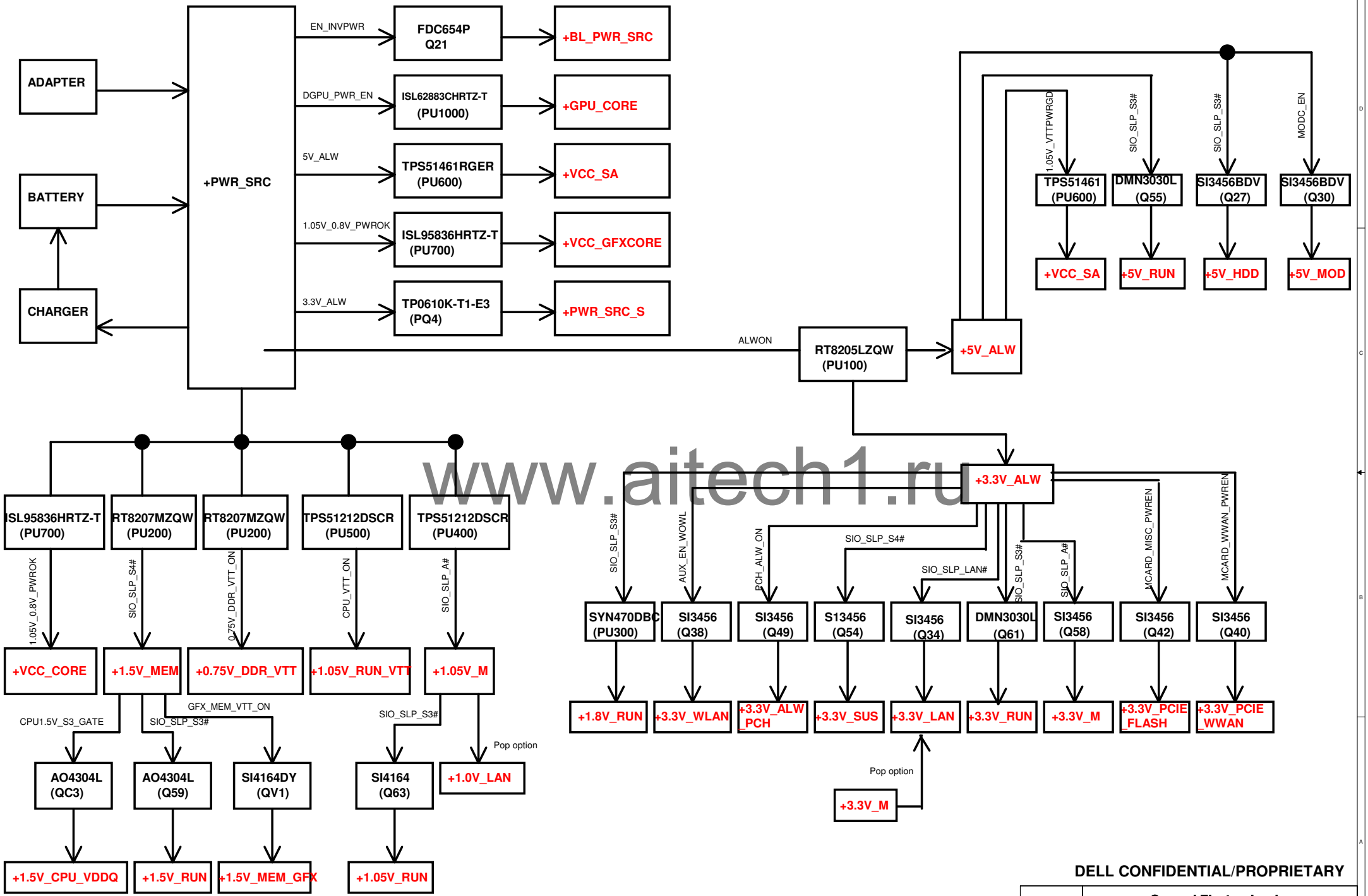

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Title: Power Rail

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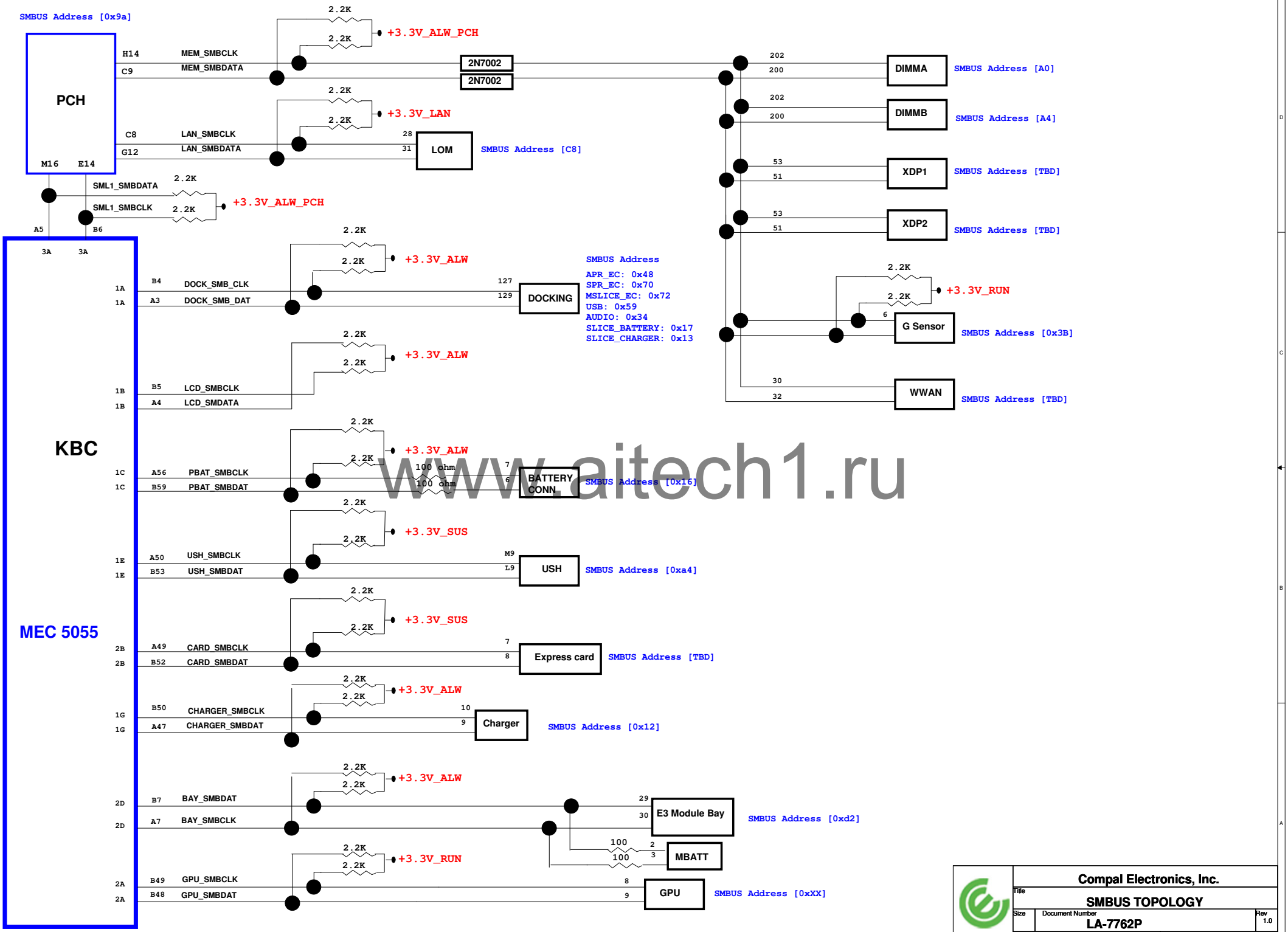

Compal Electronics, Inc.

Title: SMBUS TOPOLOGY

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(1)PEG_RCOMPO (H22) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC2.
(2)PEG_ICOMPO use 12mil connect to RC2

+1.05V_RUN_VTT

RC2
24.9_0402_1%~D

JCPU1A

CONN@

PEG_ICOMPI J22 — PEG_COMP
PEG_ICOMPO J21
PEG_RCOMPO H22

DMI

DMI_CRX_PTX_N0	B27	DMI_RX#[0]	
DMI_CRX_PTX_N1	B25	DMI_RX#[1]	
DMI_CRX_PTX_N2	A25	DMI_RX#[2]	
DMI_CRX_PTX_N3	B24	DMI_RX#[3]	
DMI_CRX_PTX_P0	B28	DMI_RX[0]	
DMI_CRX_PTX_P1	B26	DMI_RX[1]	
DMI_CRX_PTX_P2	A24	DMI_RX[2]	
DMI_CRX_PTX_P3	B23	DMI_RX[3]	
DMI_CTX_PRX_N0	G21	DMI_TX#[0]	
DMI_CTX_PRX_N1	E22	DMI_TX#[1]	
DMI_CTX_PRX_N2	F21	DMI_TX#[2]	
DMI_CTX_PRX_N3	D21	DMI_TX#[3]	
DMI_CTX_PRX_P0	G22	DMI_TX[0]	
DMI_CTX_PRX_P1	D22	DMI_TX[1]	
DMI_CTX_PRX_P2	F20	DMI_TX[2]	
DMI_CTX_PRX_P3	C21	DMI_TX[3]	

Intel(R) FDI

FDI_CTX_PRX_N0	A21	FDI0_TX#[0]	
FDI_CTX_PRX_N1	H19	FDI0_TX#[1]	
FDI_CTX_PRX_N2	E19	FDI0_TX#[2]	
FDI_CTX_PRX_N3	F18	FDI0_TX#[3]	
FDI_CTX_PRX_N4	B21	FDI1_TX#[0]	
FDI_CTX_PRX_N5	C20	FDI1_TX#[1]	
FDI_CTX_PRX_N6	D18	FDI1_TX#[2]	
FDI_CTX_PRX_N7	E17	FDI1_TX#[3]	
FDI_CTX_PRX_P0	A22	FDI0_TX[0]	
FDI_CTX_PRX_P1	G19	FDI0_TX[1]	
FDI_CTX_PRX_P2	E20	FDI0_TX[2]	
FDI_CTX_PRX_P3	G18	FDI0_TX[3]	
FDI_CTX_PRX_P4	B20	FDI1_TX[0]	
FDI_CTX_PRX_P5	C19	FDI1_TX[1]	
FDI_CTX_PRX_P6	D19	FDI1_TX[2]	
FDI_CTX_PRX_P7	F17	FDI1_TX[3]	
FDI_FSYNC0	J18	FDI0_FSYNC	
FDI_FSYNC1	J17	FDI1_FSYNC	
FDI_INT	H20	FDI_INT	
FDI_LSYNC0	J19	FDI0_LSYNC	
FDI_LSYNC1	H17	FDI1_LSYNC	

(1) EDP_COMPIO use 4mil trace to RC1
(2) EDP_ICOMPO use 12mil to RC1

eDP

EDP_COMP	A18	eDP_COMPIO	
	A17	eDP_ICOMPO	
	B16	eDP_HPD#	
	C15	eDP_AUX	
	D15	eDP_AUX#	
	C17	eDP_TX[0]	
	F16	eDP_TX[1]	
	C16	eDP_TX[2]	
	G15	eDP_TX[3]	
	C18	eDP_TX#[0]	
	E16	eDP_TX#[1]	
	D16	eDP_TX#[2]	
	F15	eDP_TX#[3]	

PCI EXPRESS* - GRAPHICS

PEG_RX#[0]	K33	PEG_CRX_GTX_N15	PEG_CRX_GTX_N[0..15] <45>
PEG_RX#[1]	M35	PEG_CRX_GTX_N14	
PEG_RX#[2]	L34	PEG_CRX_GTX_N13	
PEG_RX#[3]	J35	PEG_CRX_GTX_N12	
PEG_RX#[4]	J32	PEG_CRX_GTX_N11	
PEG_RX#[5]	H34	PEG_CRX_GTX_N10	
PEG_RX#[6]	H31	PEG_CRX_GTX_N9	
PEG_RX#[7]	G33	PEG_CRX_GTX_N8	
PEG_RX#[8]	G30	PEG_CRX_GTX_N7	
PEG_RX#[9]	F35	PEG_CRX_GTX_N6	
PEG_RX#[10]	E34	PEG_CRX_GTX_N5	
PEG_RX#[11]	E32	PEG_CRX_GTX_N4	
PEG_RX#[12]	D33	PEG_CRX_GTX_N3	
PEG_RX#[13]	D31	PEG_CRX_GTX_N2	
PEG_RX#[14]	B33	PEG_CRX_GTX_N1	
PEG_RX#[15]	C32	PEG_CRX_GTX_N0	
PEG_RX[0]	J33	PEG_CRX_GTX_P15	PEG_CRX_GTX_P[0..15] <45>
PEG_RX[1]	L35	PEG_CRX_GTX_P14	
PEG_RX[2]	K34	PEG_CRX_GTX_P13	
PEG_RX[3]	H35	PEG_CRX_GTX_P12	
PEG_RX[4]	H32	PEG_CRX_GTX_P11	
PEG_RX[5]	G34	PEG_CRX_GTX_P10	
PEG_RX[6]	G31	PEG_CRX_GTX_P9	
PEG_RX[7]	F33	PEG_CRX_GTX_P8	
PEG_RX[8]	F30	PEG_CRX_GTX_P7	
PEG_RX[9]	E35	PEG_CRX_GTX_P6	
PEG_RX[10]	E33	PEG_CRX_GTX_P5	
PEG_RX[11]	F32	PEG_CRX_GTX_P4	
PEG_RX[12]	D34	PEG_CRX_GTX_P3	
PEG_RX[13]	E31	PEG_CRX_GTX_P2	
PEG_RX[14]	C33	PEG_CRX_GTX_P1	
PEG_RX[15]	B32	PEG_CRX_GTX_P0	
PEG_TX#[0]	M29	PEG_CTX_GRX_C_N15	
PEG_TX#[1]	M32	PEG_CTX_GRX_C_N14	
PEG_TX#[2]	M31	PEG_CTX_GRX_C_N13	
PEG_TX#[3]	L32	PEG_CTX_GRX_C_N12	
PEG_TX#[4]	L29	PEG_CTX_GRX_C_N11	
PEG_TX#[5]	K31	PEG_CTX_GRX_C_N10	
PEG_TX#[6]	K28	PEG_CTX_GRX_C_N9	
PEG_TX#[7]	J30	PEG_CTX_GRX_C_N8	
PEG_TX#[8]	J28	PEG_CTX_GRX_C_N7	
PEG_TX#[9]	H29	PEG_CTX_GRX_C_N6	
PEG_TX#[10]	G27	PEG_CTX_GRX_C_N5	
PEG_TX#[11]	E29	PEG_CTX_GRX_C_N4	
PEG_TX#[12]	F27	PEG_CTX_GRX_C_N3	
PEG_TX#[13]	D28	PEG_CTX_GRX_C_N2	
PEG_TX#[14]	F26	PEG_CTX_GRX_C_N1	
PEG_TX#[15]	E25	PEG_CTX_GRX_C_N0	
PEG_TX[0]	M28	PEG_CTX_GRX_C_P15	
PEG_TX[1]	M33	PEG_CTX_GRX_C_P14	
PEG_TX[2]	M30	PEG_CTX_GRX_C_P13	
PEG_TX[3]	L31	PEG_CTX_GRX_C_P12	
PEG_TX[4]	L28	PEG_CTX_GRX_C_P11	
PEG_TX[5]	K30	PEG_CTX_GRX_C_P10	
PEG_TX[6]	K27	PEG_CTX_GRX_C_P9	
PEG_TX[7]	J29	PEG_CTX_GRX_C_P8	
PEG_TX[8]	J27	PEG_CTX_GRX_C_P7	
PEG_TX[9]	H28	PEG_CTX_GRX_C_P6	
PEG_TX[10]	G28	PEG_CTX_GRX_C_P5	
PEG_TX[11]	E28	PEG_CTX_GRX_C_P4	
PEG_TX[12]	F28	PEG_CTX_GRX_C_P3	
PEG_TX[13]	D27	PEG_CTX_GRX_C_P2	
PEG_TX[14]	E26	PEG_CTX_GRX_C_P1	
PEG_TX[15]	D25	PEG_CTX_GRX_C_P0	

TYCO_2013620-3_IVYBRIDGE

PEG_CTX_GRX_P[0..15] — PEG_CTX_GRX_P[0..15] <45>
PEG_CTX_GRX_N[0..15] — PEG_CTX_GRX_N[0..15] <45>

Check if support PCIE GEN2

PEG_CTX_GRX_C_P0	CC1	2	1	0.22U_0402_16V7K~D	PEG_CTX_GRX_P0
PEG_CTX_GRX_C_N0	CC2	2	1	0.22U_0402_16V7K~D	PEG_CTX_GRX_N0
PEG_CTX_GRX_C_P1	CC3	2	1	0.22U_0402_16V7K~D	PEG_CTX_GRX_P1
PEG_CTX_GRX_C_N1	CC4	2	1	0.22U_0402_16V7K~D	PEG_CTX_GRX_N1
PEG_CTX_GRX_C_P2	CC5	2	1	0.22U_0402_16V7K~D	PEG_CTX_GRX_P2
PEG_CTX_GRX_C_N2	CC6	2	1	0.22U_0402_16V7K~D	PEG_CTX_GRX_N2
PEG_CTX_GRX_C_P3	CC7	2	1	0.22U_0402_16V7K~D	PEG_CTX_GRX_P3
PEG_CTX_GRX_C_N3	CC8	2	1	0.22U_0402_16V7K~D	PEG_CTX_GRX_N3
PEG_CTX_GRX_C_P4	CC9	2	1	0.22U_0402_16V7K~D	PEG_CTX_GRX_P4
PEG_CTX_GRX_C_N4	CC10	2	1	0.22U_0402_16V7K~D	PEG_CTX_GRX_N4
PEG_CTX_GRX_C_P5	CC11	2	1	0.22U_0402_16V7K~D	PEG_CTX_GRX_P5
PEG_CTX_GRX_C_N5	CC12	2	1	0.22U_0402_16V7K~D	PEG_CTX_GRX_N5
PEG_CTX_GRX_C_P6	CC13	2	1	0.22U_0402_16V7K~D	PEG_CTX_GRX_P6
PEG_CTX_GRX_C_N6	CC14	2	1	0.22U_0402_16V7K~D	PEG_CTX_GRX_N6
PEG_CTX_GRX_C_P7	CC15	2	1	0.22U_0402_16V7K~D	PEG_CTX_GRX_P7
PEG_CTX_GRX_C_N7	CC16	2	1	0.22U_0402_16V7K~D	PEG_CTX_GRX_N7
PEG_CTX_GRX_C_P8	CC17	1	2	0.22U_0402_16V7K~D	PEG_CTX_GRX_P8
PEG_CTX_GRX_C_N8	CC18	1	2	0.22U_0402_16V7K~D	PEG_CTX_GRX_N8
PEG_CTX_GRX_C_P9	CC19	1	2	0.22U_0402_16V7K~D	PEG_CTX_GRX_P9
PEG_CTX_GRX_C_N9	CC20	1	2	0.22U_0402_16V7K~D	PEG_CTX_GRX_N9
PEG_CTX_GRX_C_P10	CC21	1	2	0.22U_0402_16V7K~D	PEG_CTX_GRX_P10
PEG_CTX_GRX_C_N10	CC22	1	2	0.22U_0402_16V7K~D	PEG_CTX_GRX_N10
PEG_CTX_GRX_C_P11	CC23	1	2	0.22U_0402_16V7K~D	PEG_CTX_GRX_P11
PEG_CTX_GRX_C_N11	CC24	1	2	0.22U_0402_16V7K~D	PEG_CTX_GRX_N11
PEG_CTX_GRX_C_P12	CC25	1	2	0.22U_0402_16V7K~D	PEG_CTX_GRX_P12
PEG_CTX_GRX_C_N12	CC26	1	2	0.22U_0402_16V7K~D	PEG_CTX_GRX_N12
PEG_CTX_GRX_C_P13	CC27	1	2	0.22U_0402_16V7K~D	PEG_CTX_GRX_P13
PEG_CTX_GRX_C_N13	CC28	1	2	0.22U_0402_16V7K~D	PEG_CTX_GRX_N13
PEG_CTX_GRX_C_P14	CC29	1	2	0.22U_0402_16V7K~D	PEG_CTX_GRX_P14
PEG_CTX_GRX_C_N14	CC30	1	2	0.22U_0402_16V7K~D	PEG_CTX_GRX_N14
PEG_CTX_GRX_C_P15	CC31	1	2	0.22U_0402_16V7K~D	PEG_CTX_GRX_P15
PEG_CTX_GRX_C_N15	CC32	1	2	0.22U_0402_16V7K~D	PEG_CTX_GRX_N15

JCPU1I — CONN@

VSS

T35	VSS161	VSS234	F22
T34	VSS162	VSS235	F19
T33	VSS163	VSS236	E30
T32	VSS164	VSS237	E27
T31	VSS165	VSS238	E24
T30	VSS166	VSS239	E21
T29	VSS167	VSS240	E18
T28	VSS168	VSS241	E15
T27	VSS169	VSS242	E13
T26	VSS170	VSS243	E10
P9	VSS171	VSS244	E9
P8	VSS172	VSS245	E8
P6	VSS173	VSS246	E7
P5	VSS174	VSS247	E6
P3	VSS175	VSS248	E5
P2	VSS176	VSS249	E4
N35	VSS177	VSS250	E3
N34	VSS178	VSS251	E2
N33	VSS179	VSS252	E1
N32	VSS180	VSS253	D35
N31	VSS181	VSS254	D32
N30	VSS182	VSS255	D29
N29	VSS183	VSS256	D26
N28	VSS184	VSS257	D20
N27	VSS185	VSS258	D17
N26	VSS186	VSS259	C34
M34	VSS187	VSS260	C31
L33	VSS188	VSS261	C28
L30	VSS189	VSS262	C27
L27	VSS190	VSS263	C25
L9	VSS191	VSS264	C23
L8	VSS192	VSS265	C10
L6	VSS193	VSS266	C1
L5	VSS194	VSS267	B22
L4	VSS195	VSS268	B19
L3	VSS196	VSS269	B17
L2	VSS197	VSS270	B15
L1	VSS198	VSS271	B13
K35	VSS199	VSS272	B11
K32	VSS200	VSS273	B9
K29	VSS201	VSS274	B8
K26	VSS202	VSS275	B7
J34	VSS203	VSS276	B5
J31	VSS204	VSS277	B3
H33	VSS205	VSS278	B2
H30	VSS206	VSS279	A35
H27	VSS207	VSS280	A32
H24	VSS208	VSS281	A29
H21	VSS209	VSS282	A26
H18	VSS210	VSS283	A23
H15	VSS211	VSS284	A20
H13	VSS212	VSS285	A3
H10	VSS213		
H9	VSS214		
H8	VSS215		
H7	VSS216		
H6	VSS217		
H5	VSS218		
H4	VSS219		
H3	VSS220		
H2	VSS221		
H1	VSS222		
G35	VSS223		
G32	VSS224		
G29	VSS225		
G26	VSS226		
G23	VSS227		
G20	VSS228		
G17	VSS229		
G11	VSS230		
F34	VSS231		
F31	VSS232		
F29	VSS233		

TYCO_2013620-3_IVYBRIDGE

DP Compensation

+1.05V_RUN_VTT

RC1
24.9_0402_1%~D

EDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Compal Electronics, Inc.

Title: Ivy Bridge (1/6)

Size | Document Number: LA-7762P | Rev: 1.0

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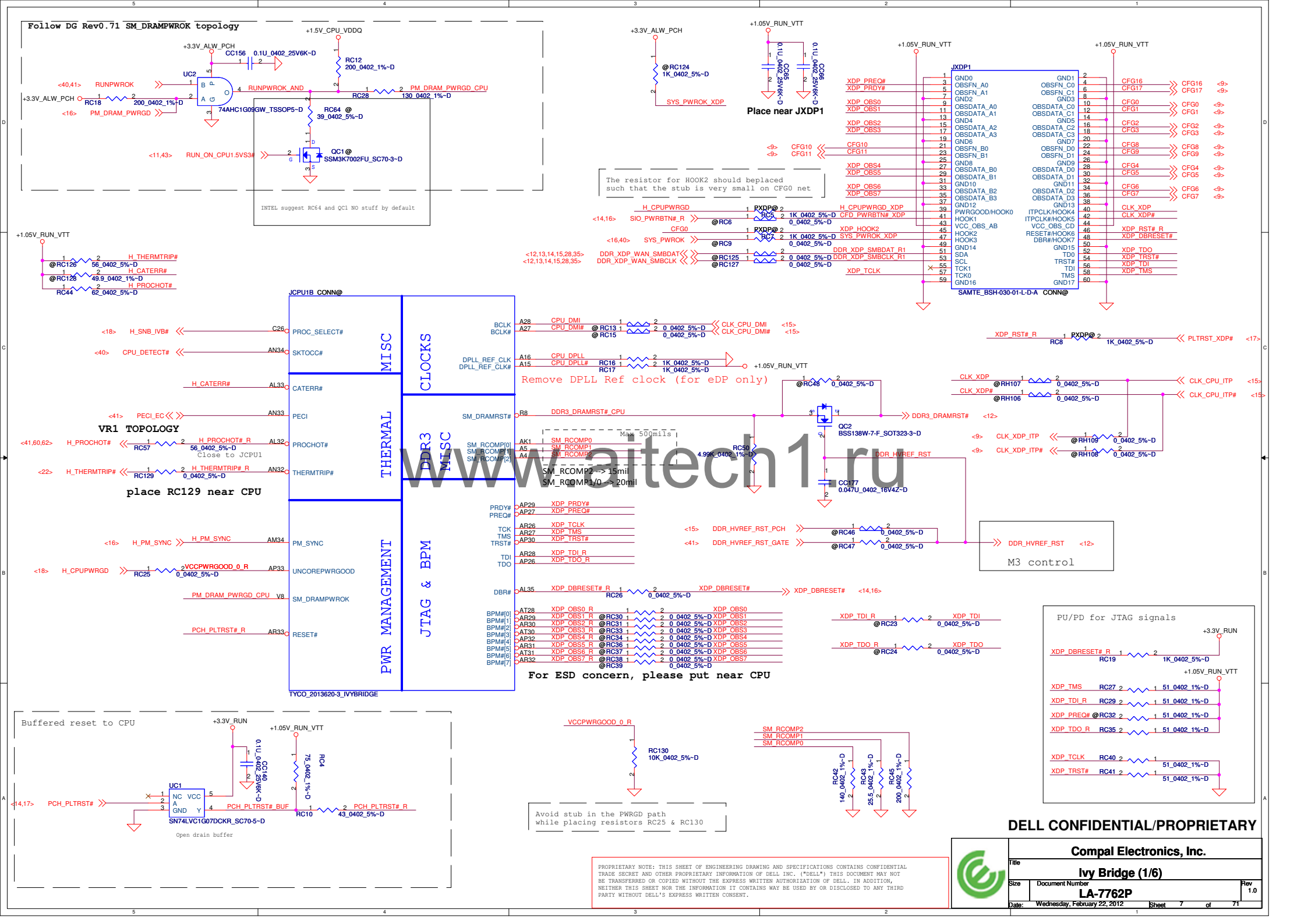
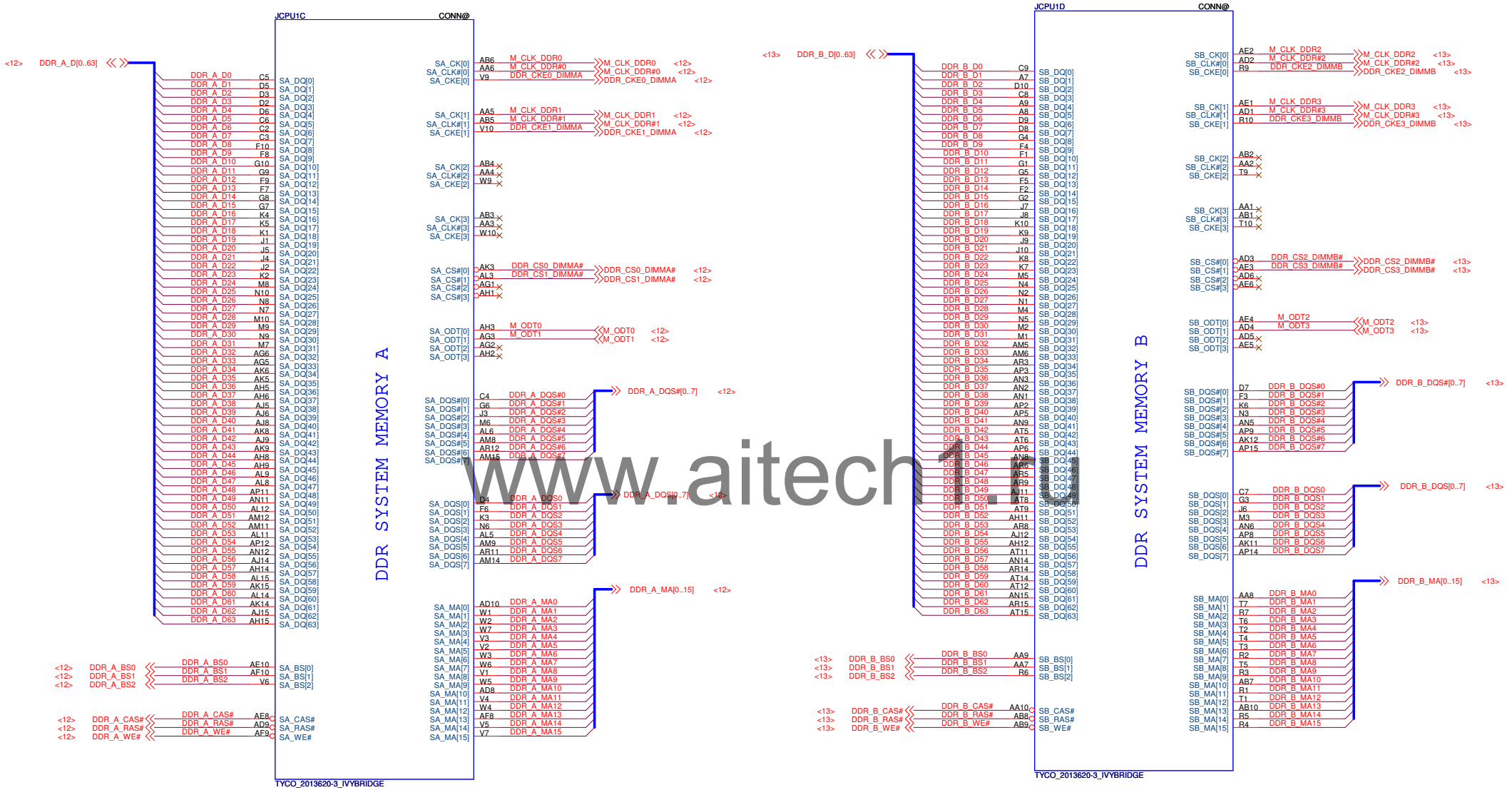


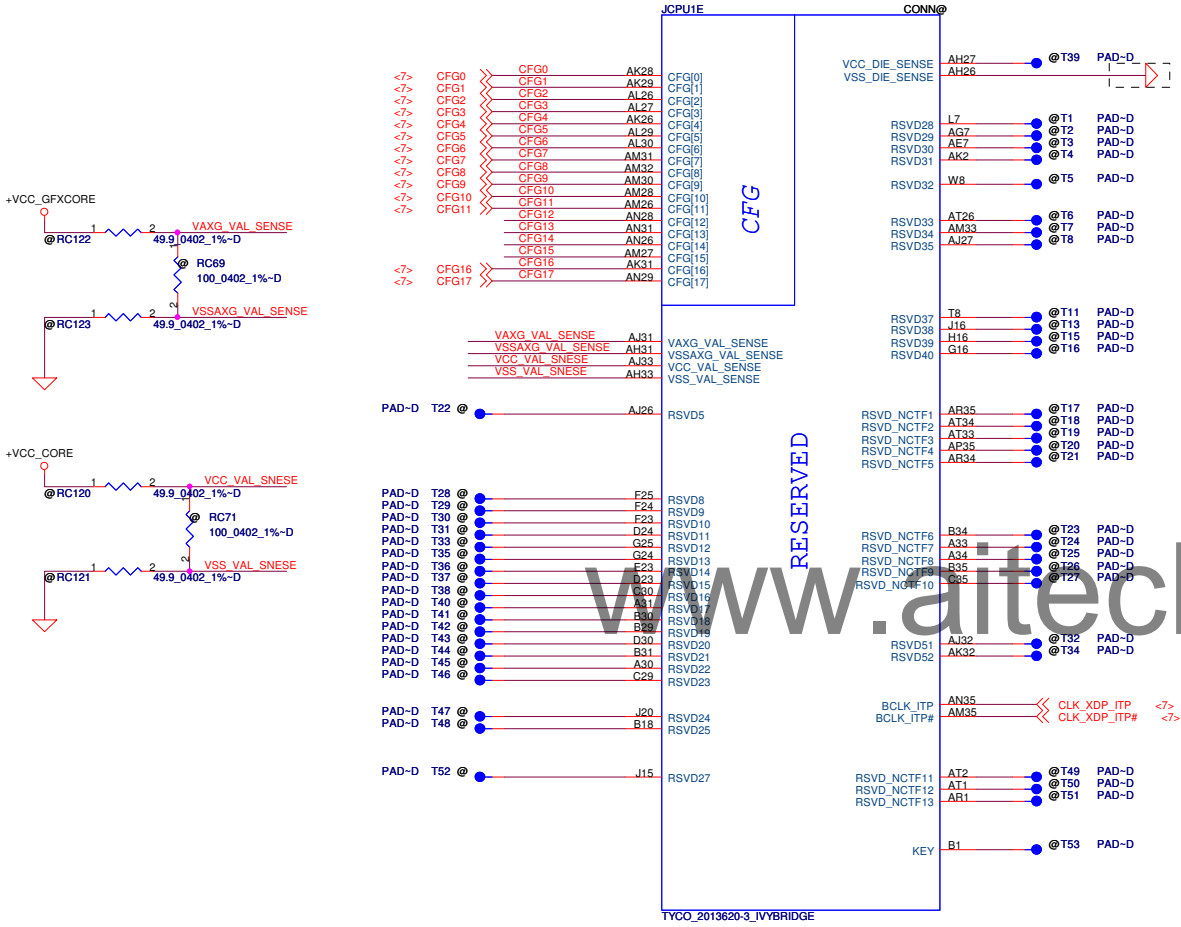


Compal Electronics, Inc.

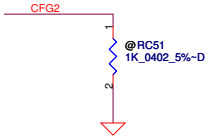
Title: Ivy Bridge (1/6)

Size | Document Number: LA-7762P | Rev: 1.0

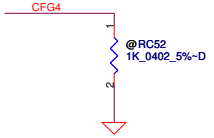
Date: Wednesday, February 22, 2012 | Sheet 8 of 71



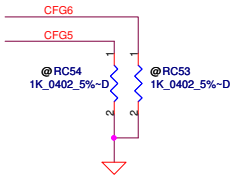
CFG Straps for Processor



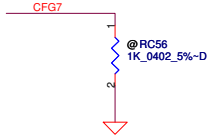
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

POWER

JCPU1F

CONN@

+VCC_CORE

94A

+1.05V_RUN_VTT

8.5A

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

AG35	VCC1	
AG34	VCC2	
AG33	VCC3	
AG32	VCC4	
AG31	VCC5	
AG30	VCC6	
AG29	VCC7	
AG28	VCC8	
AG27	VCC9	
AG26	VCC10	
AF35	VCC11	
AF34	VCC12	
AF33	VCC13	
AF32	VCC14	
AF31	VCC15	
AF30	VCC16	
AF29	VCC17	
AF28	VCC18	
AF27	VCC19	
AF26	VCC20	
AD35	VCC21	
AD34	VCC22	
AD33	VCC23	
AD32	VCC24	
AD31	VCC25	
AD30	VCC26	
AD29	VCC27	
AD28	VCC28	
AD27	VCC29	
AD26	VCC30	
AC35	VCC31	
AC34	VCC32	
AC33	VCC33	
AC32	VCC34	
AC31	VCC35	
AC30	VCC36	
AC29	VCC37	
AC28	VCC38	
AC27	VCC39	
AC26	VCC40	
AA35	VCC41	
AA34	VCC42	
AA33	VCC43	
AA32	VCC44	
AA31	VCC45	
AA30	VCC46	
AA29	VCC47	
AA28	VCC48	
AA27	VCC49	
AA26	VCC50	
Y35	VCC51	
Y34	VCC52	
Y33	VCC53	
Y32	VCC54	
Y31	VCC55	
Y30	VCC56	
Y29	VCC57	
Y28	VCC58	
Y27	VCC59	
Y26	VCC60	
V35	VCC61	
V34	VCC62	
V33	VCC63	
V32	VCC64	
V31	VCC65	
V30	VCC66	
V29	VCC67	
V28	VCC68	
V27	VCC69	
V26	VCC70	
U35	VCC71	
U34	VCC72	
U33	VCC73	
U32	VCC74	
U31	VCC75	
U30	VCC76	
U29	VCC77	
U28	VCC78	
U27	VCC79	
U26	VCC80	
R35	VCC81	
R34	VCC82	
R33	VCC83	
R32	VCC84	
R31	VCC85	
R30	VCC86	
R29	VCC87	
R28	VCC88	
R27	VCC89	
R26	VCC90	
P35	VCC91	
P34	VCC92	
P33	VCC93	
P32	VCC94	
P31	VCC95	
P30	VCC96	
P29	VCC97	
P28	VCC98	
P27	VCC99	
P26	VCC100	

VCCIO1	AH13
VCCIO2	AH10
VCCIO3	AG10
VCCIO4	AC10
VCCIO5	Y10
VCCIO6	U10
VCCIO7	P10
VCCIO8	L10
VCCIO9	J14
VCCIO10	J13
VCCIO11	J12
VCCIO12	J11
VCCIO13	H14
VCCIO14	H12
VCCIO15	H11
VCCIO16	G14
VCCIO17	G13
VCCIO18	G12
VCCIO19	F14
VCCIO20	F13
VCCIO21	F12
VCCIO22	F11
VCCIO23	E14
VCCIO24	E12
VCCIO25	E11
VCCIO26	D14
VCCIO27	D13
VCCIO28	D12
VCCIO29	D11
VCCIO30	C14
VCCIO31	C13
VCCIO32	C12
VCCIO33	C11
VCCIO34	B14
VCCIO35	B12
VCCIO36	A14
VCCIO37	A13
VCCIO38	A12
VCCIO39	A11
VCCIO40	J23

Note: Place the PU resistors close to CPU
RC61 close to CPU 300 - 1500mils

+1.05V_RUN_VTT

RC60
75_0402_1%~D

H_CPU_SVIDALRT#

RC61
43_0402_5%~D

VIDALERT_N <60>

+1.05V_RUN_VTT

RC63
130_0402_1%~D

CAD Note: Place the PU
resistors close to CPU
RC63 close to CPU 300 - 1500mils

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 VIDSCLK VIDSCLK <60>
VIDSOUT AJ28 VIDSOUT VIDSOUT <60>

H_CPU_SVIDALRT# must be routed between the VIDSOUT and VIDSCLK lines to reduce cross talk. 18 mils spacing to others.

+VCC_CORE

Place RC66, RC70near CPU

@RC75
100_0402_1%~D

RC66
100_0402_1%~D

VCC_SENSE AJ35 VCCSENSE_R
VSS_SENSE AJ34 VSSSENSE_R

@RC67 0_0402_5%~D
@RC68 0_0402_5%~D

VCCSENSE <60>
VSSSENSE <60>

RC98
10_0402_1%~D

+1.05V_RUN_VTT

VCCIO_SENSE B10 VTT_SENSE
VSS_SENSE_VCCIO A10 VSSIO_SENSE_R

VTT_SENSE <58>
VSSIO_SENSE_R <58>

RC70
100_0402_1%~D

RC133
10_0402_1%~D

Iccmax current changed for PDDG Rev0.7

CPU Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05	8.5
VAXG	0.0-1.1	26
VCCPLL	1.8	3
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 ★

★ Description

5A to Mem controller(+1.5V_CPU_VDDQ)
5-6A to 2 DIMMs/channel
2-5A to +1.5V_RUN & +0.75V_DDR_VTT

TYCO_2013620-3_IVYBRIDGE

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Compal Electronics, Inc.

Title: Ivy Bridge (1/6)

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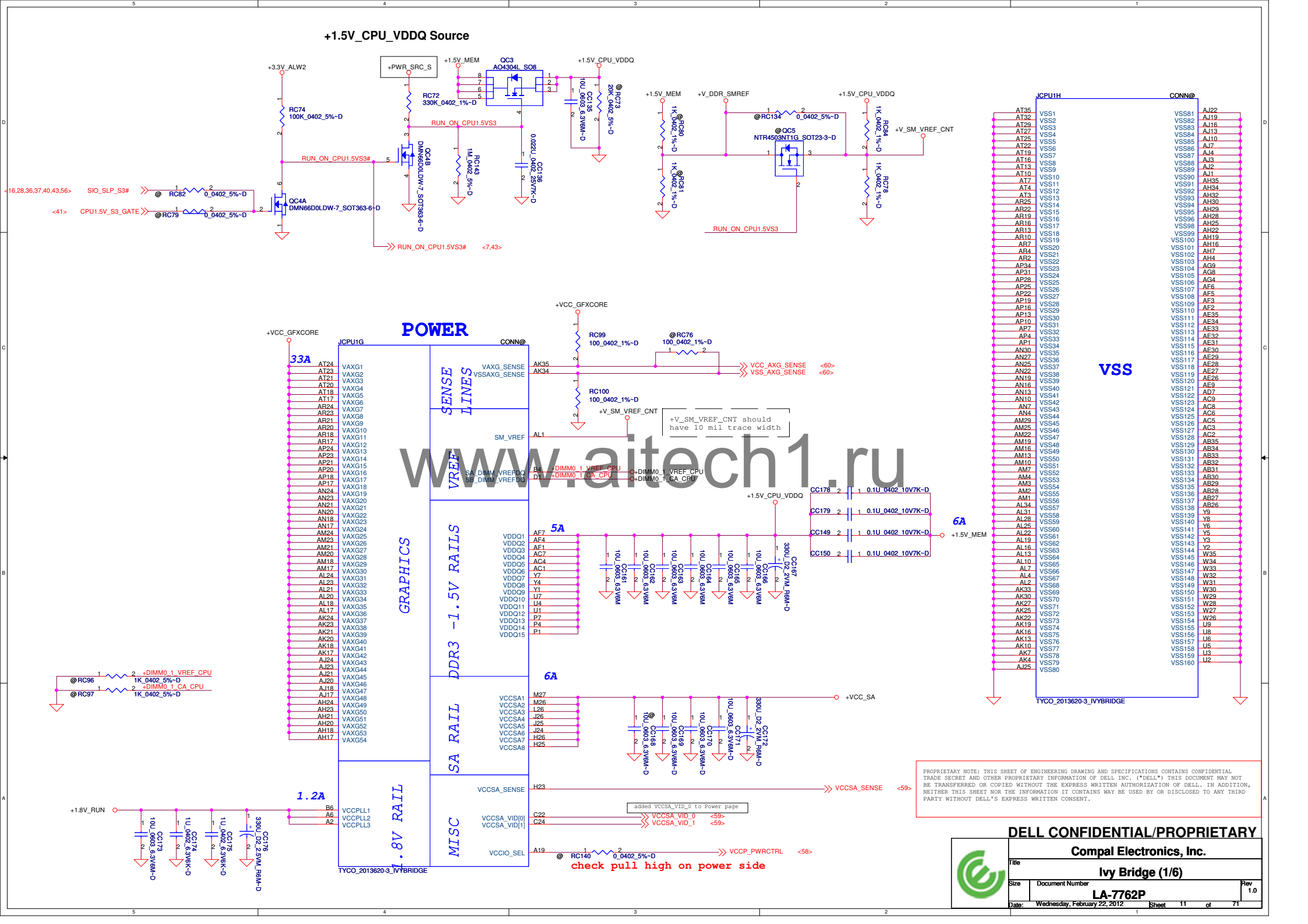

JDIMM1 H=5.2

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM1

Layout Note: Place near JDIMM1.203,204

JDIMM1_CONN@

TYCO_2-2013289-2~D

M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

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Title	DDRIII-SODIMM SLOT1
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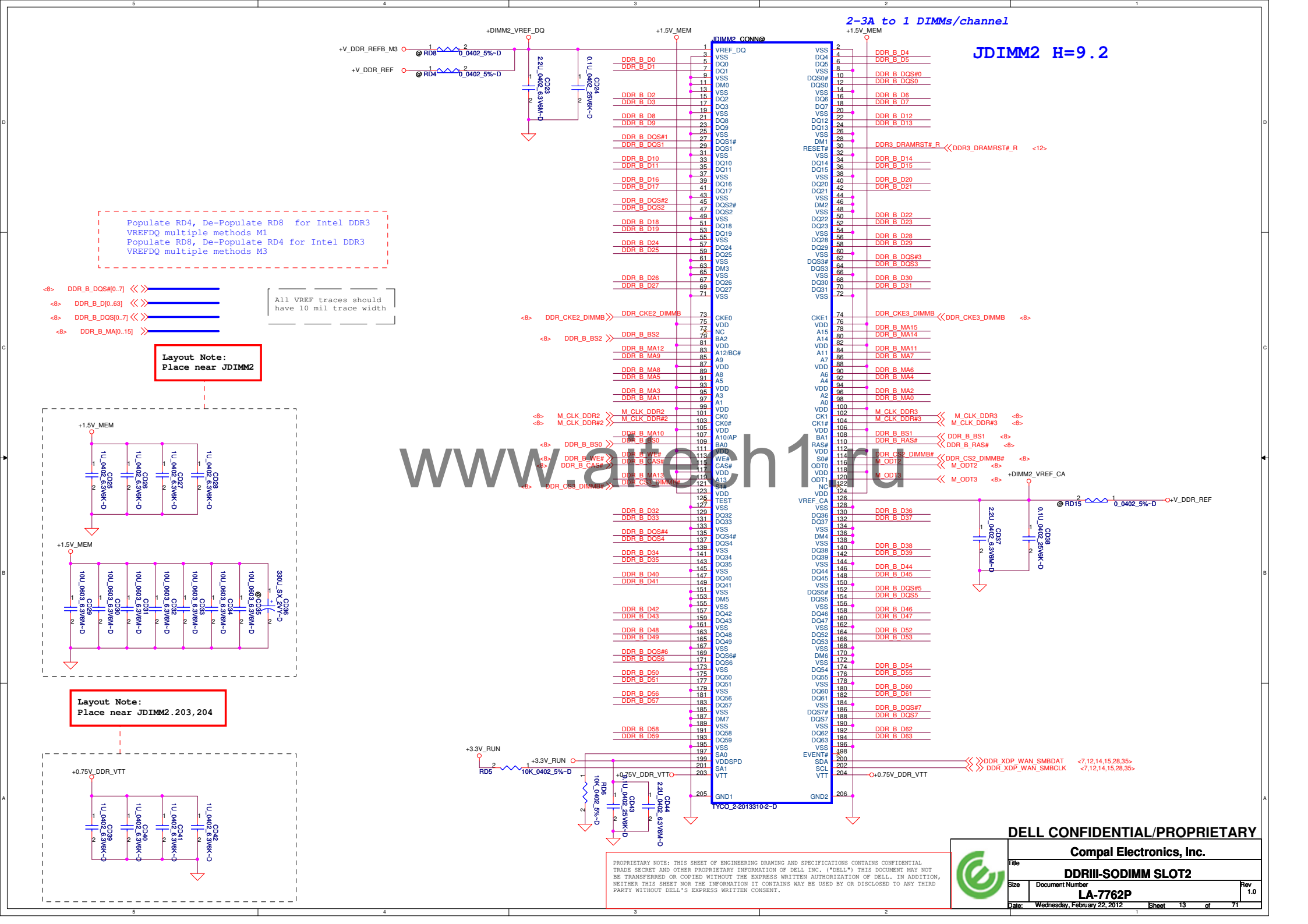

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

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CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

INTVRMEN- Integrated SUS 1.1V VRM Enable
* High - Enable Internal VRs
Low - Enable External VRs

On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low

CMOS place near DIMM

Follow INTEL CRB 0.7

INTEL HDA_SYNC isolation circuit

200 MIL SO8
64Mb Flash ROM

200 MIL SO8
32Mb Flash ROM

HDD

ODD/ E Module Bay

E-SATA

DOCK

No Reboot Strap
SPKR: Low = Default; High = No Reboot

BBS_BIT0 - BIOS BOOT STRAP BIT 0

Compal Electronics, Inc.

Title: PCH (1/8)

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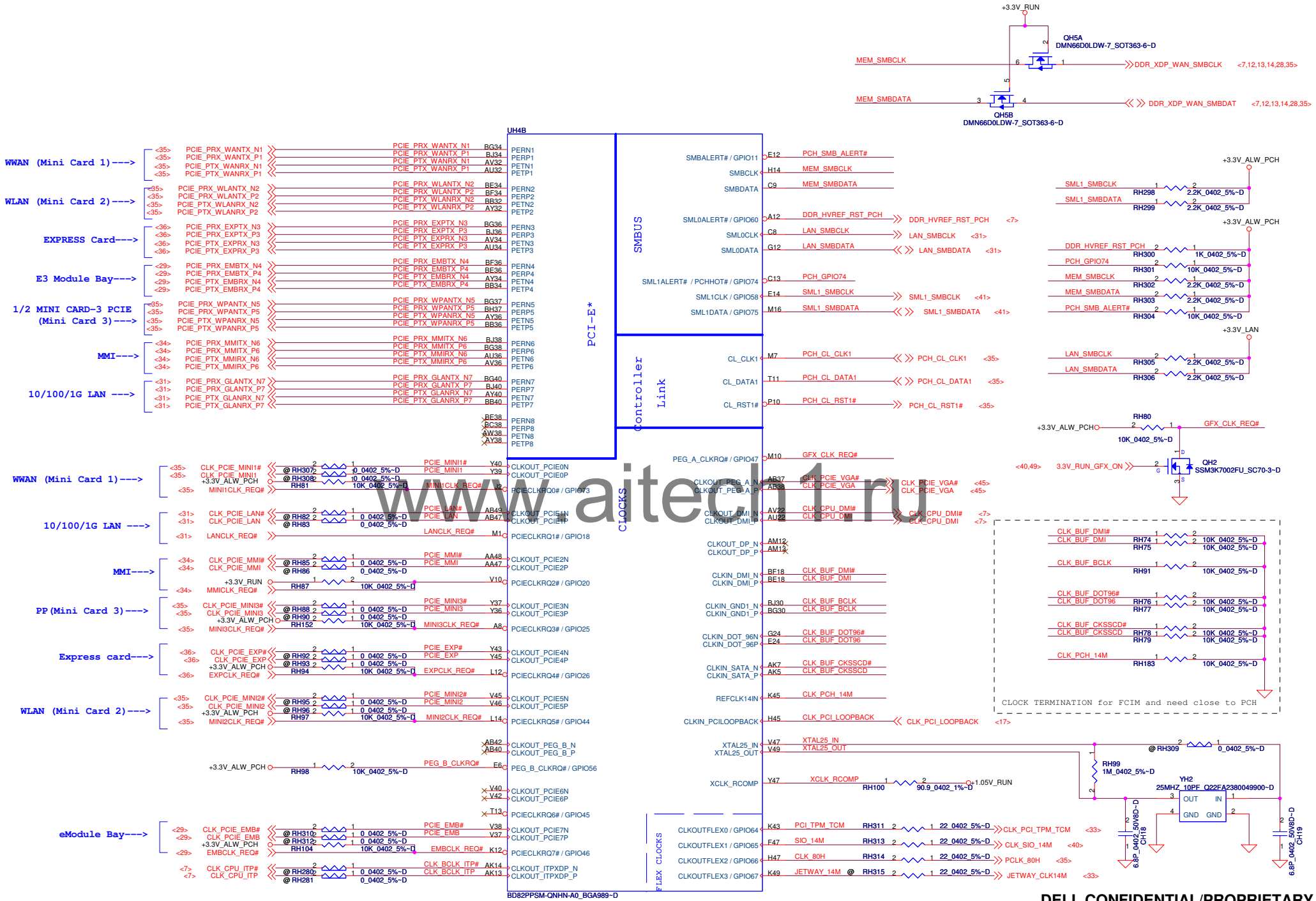

PCIE REQ power rail:
suspend: 0 3 4 5 6 7
core: 1 2

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Compal Electronics, Inc.	
Title	PCH (2/8)
Size	Document Number: LA-7762P
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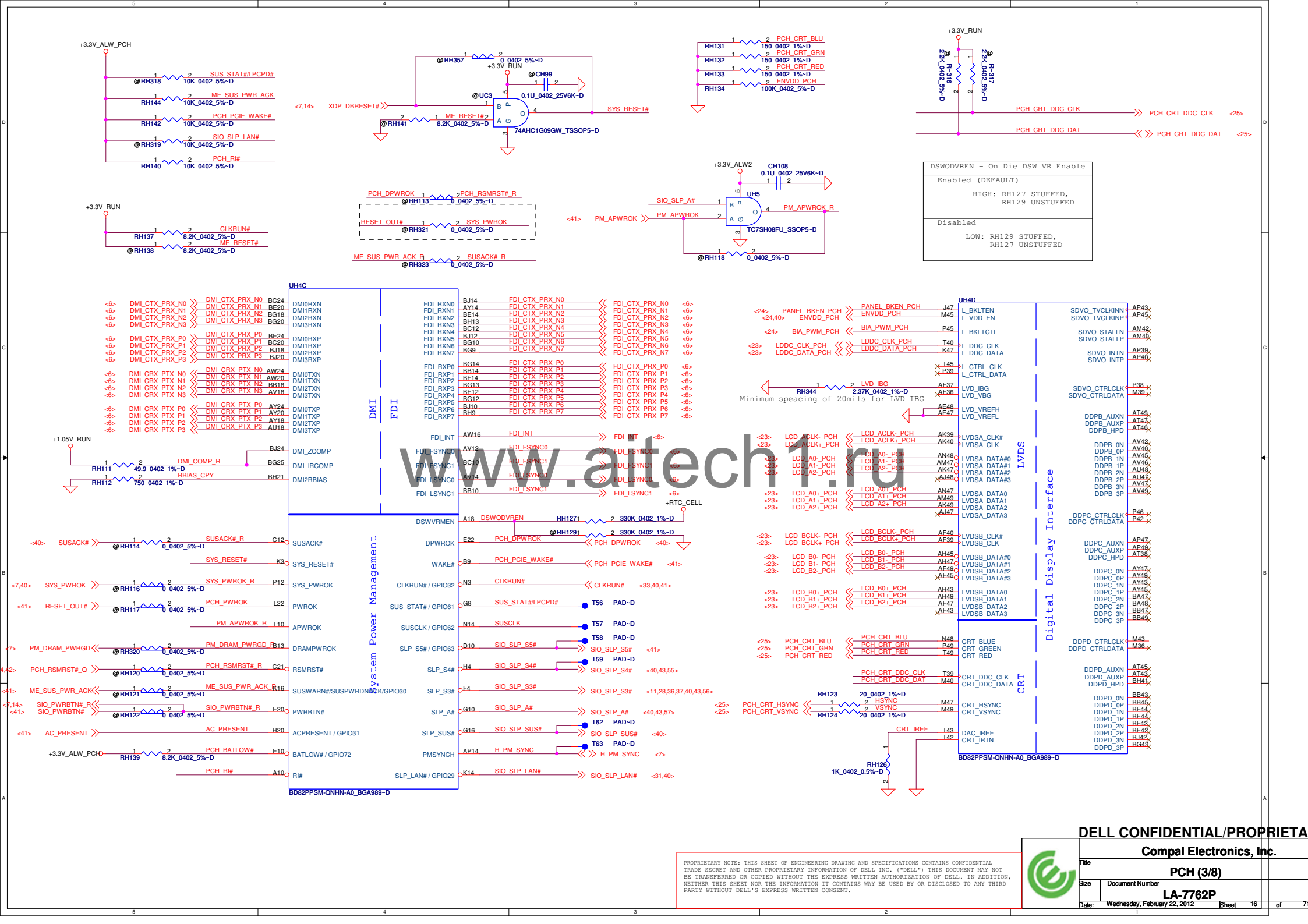

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Title: PCH (3/8)

Size: | Document Number: LA-7762P

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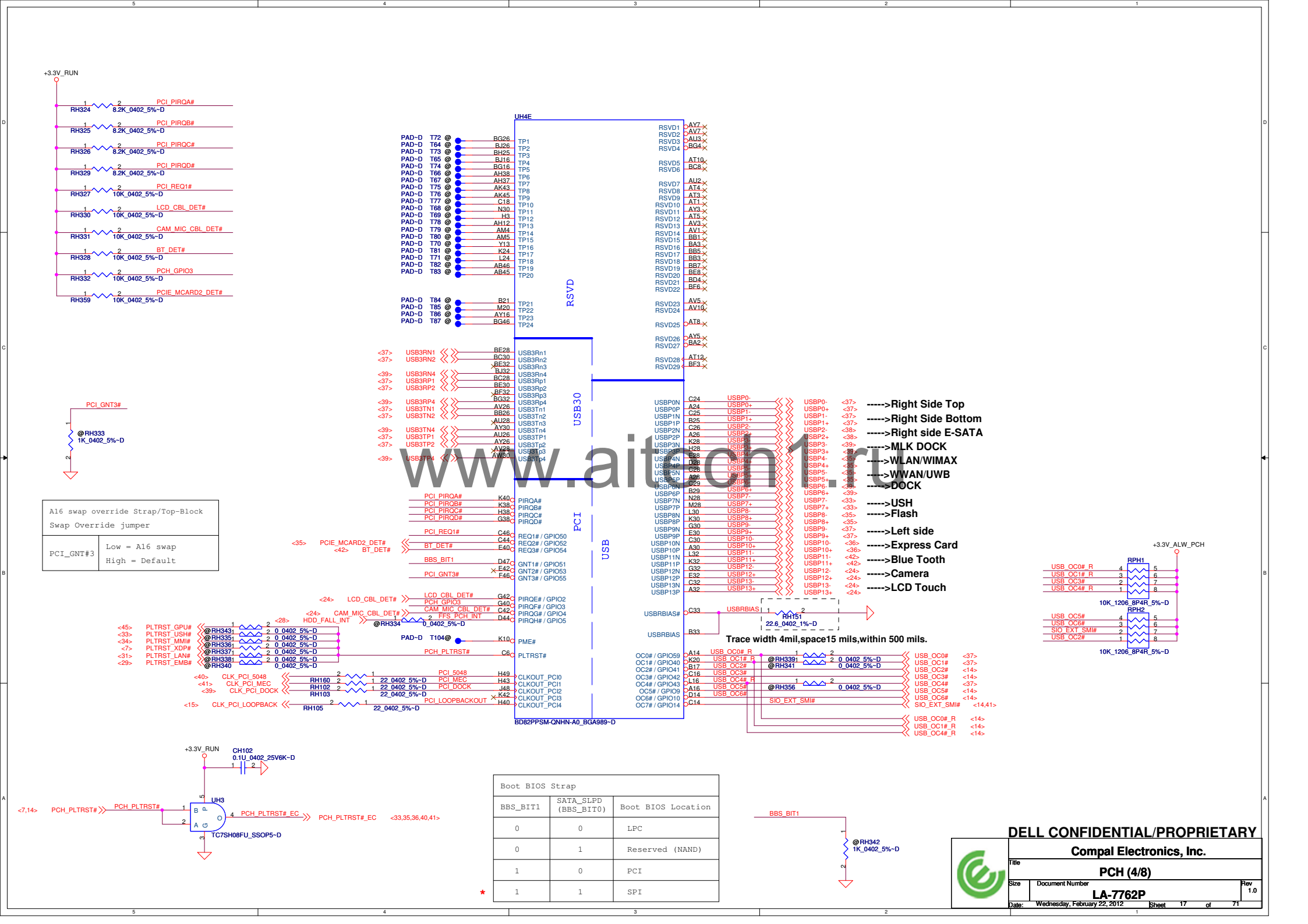

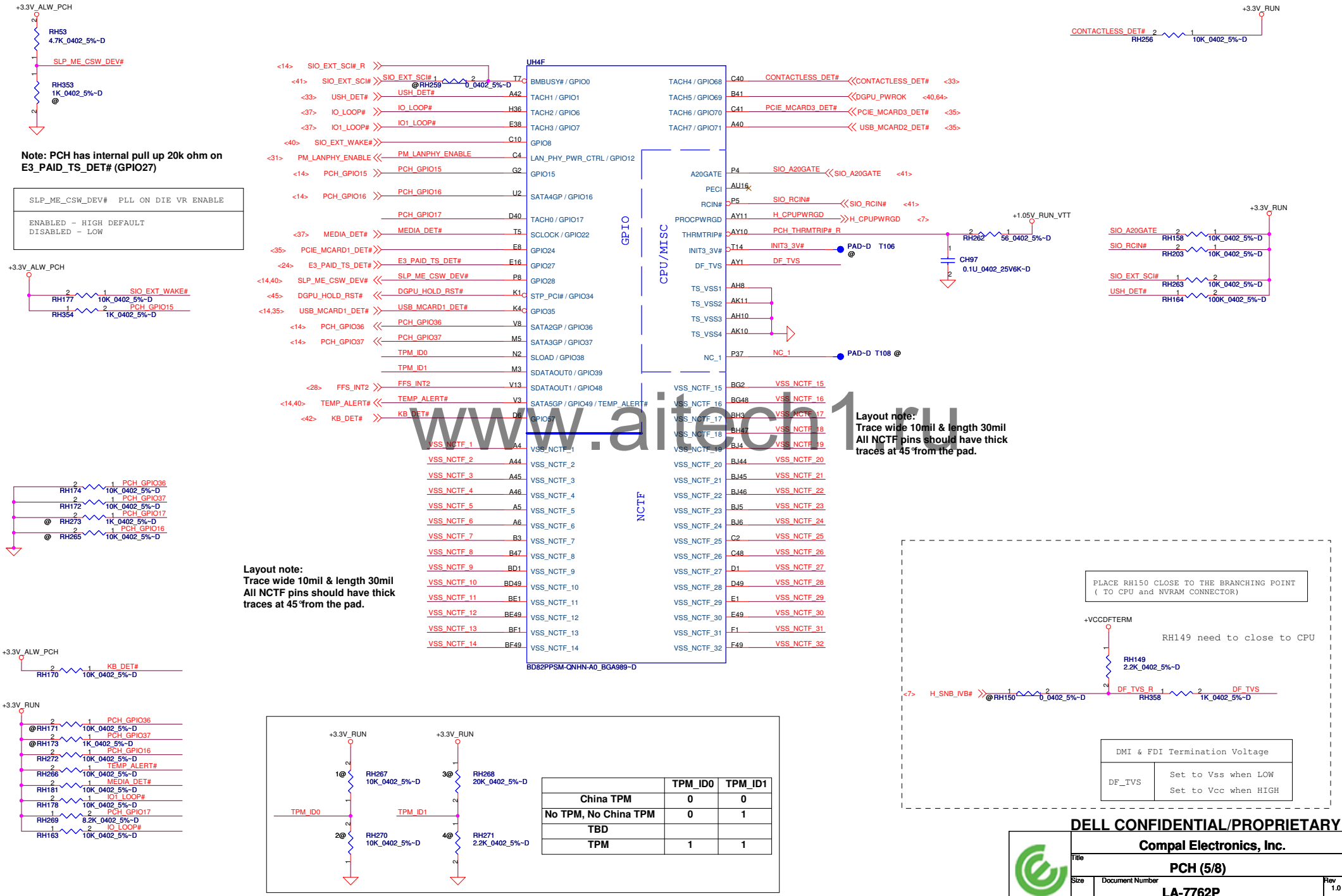

	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
TBD		
TPM	1	1

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Compal Electronics, Inc.

Title: PCH (5/8)

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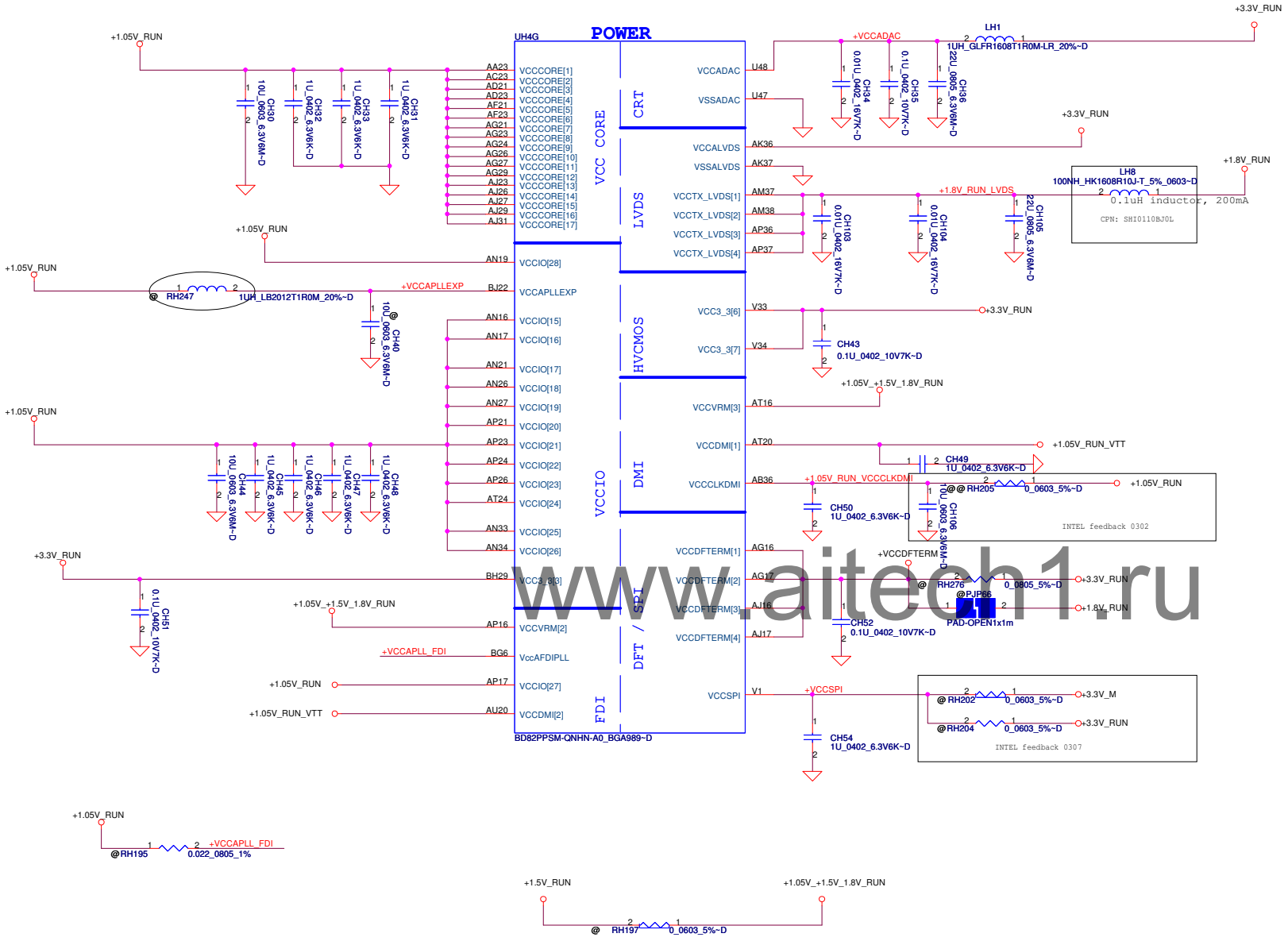

PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.288
VccADAC3	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.05	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VCCDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.126
VccSusHDA	3.3	0.01
VccVRM	1.8 / 1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

Compal Electronics, Inc.

Title: PCH (6/8)

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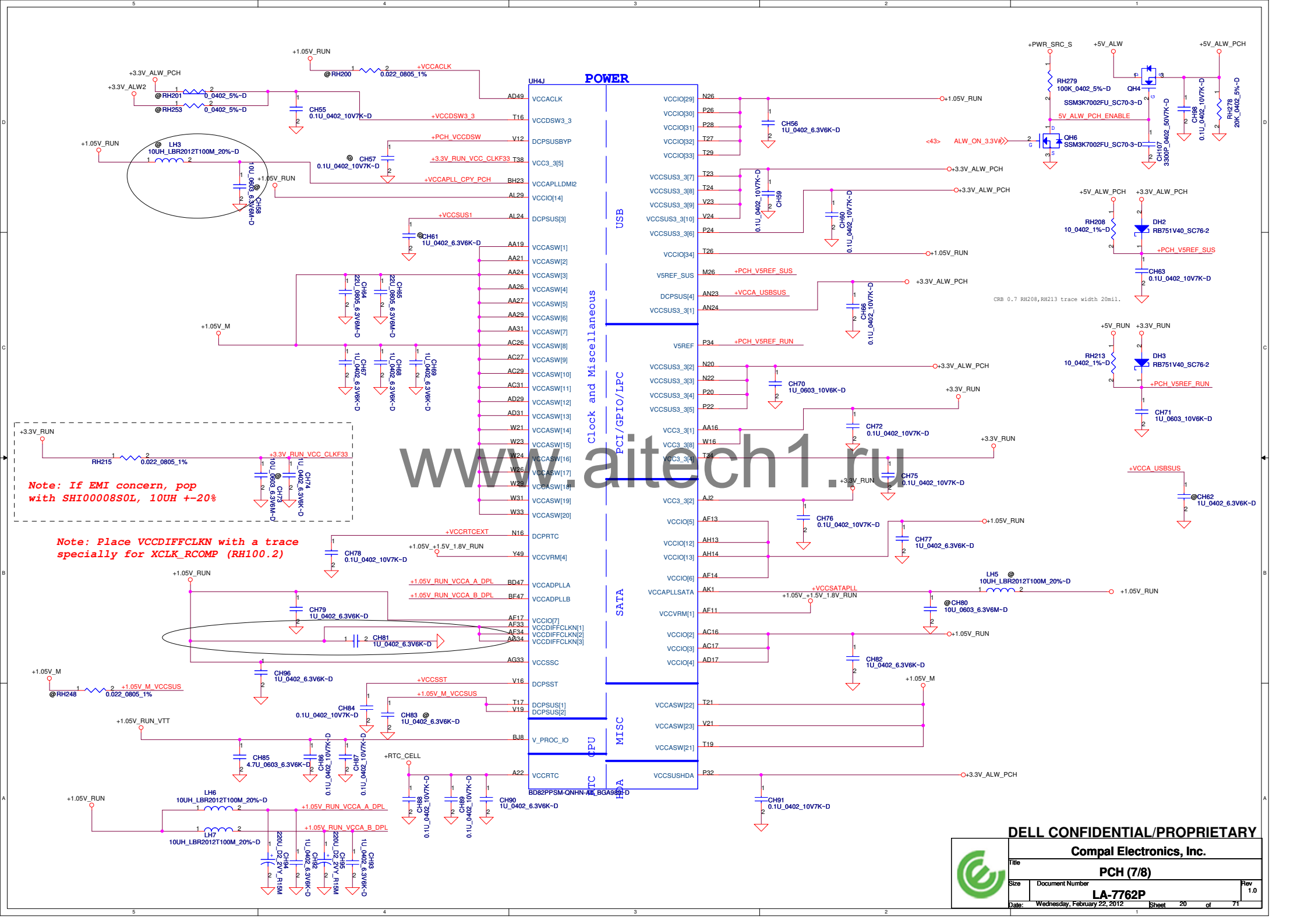
POWER
UH4J
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
HDA
Note: If EMI concern, pop with SHI00008S0L, 10UH +-20%
Note: Place VCCDIFFCLKN with a trace specially for XCLK_RCOMP (RH100.2)
BD82PPSM-QNHN-A0_BGA989-D
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Compal Electronics, Inc.
PCH (7/8)
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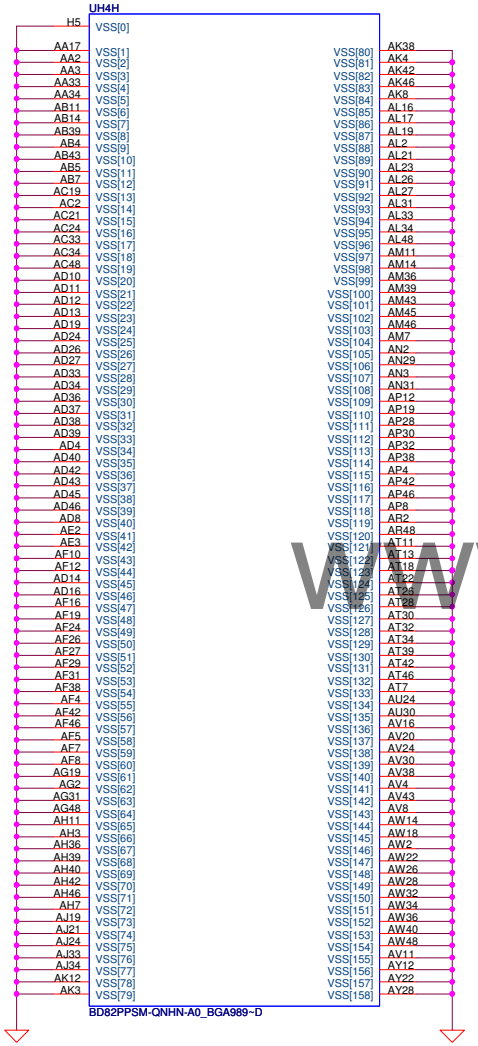

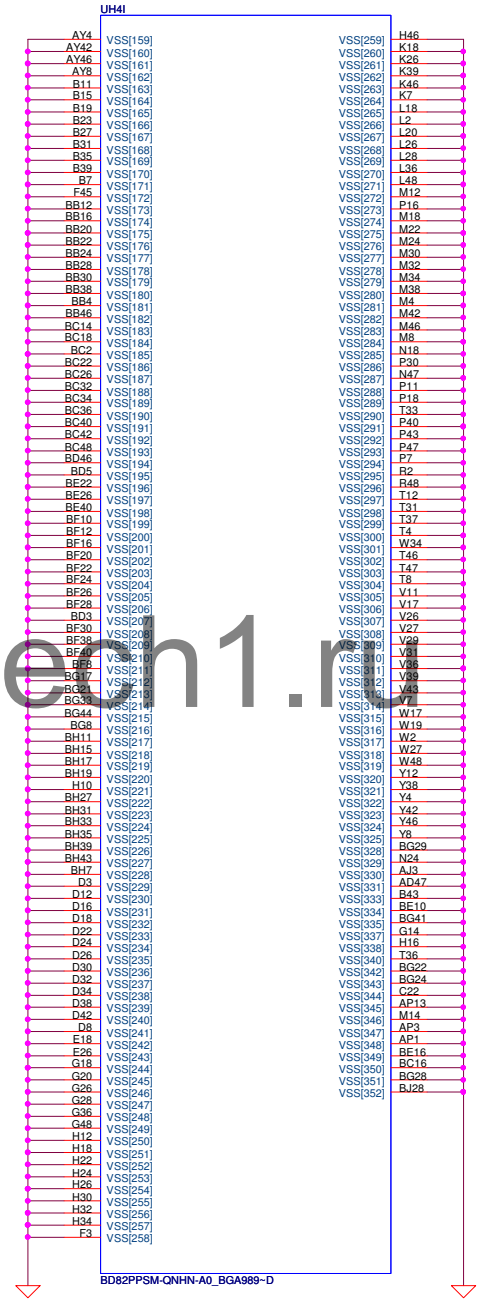

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Title	PCH (8/8)
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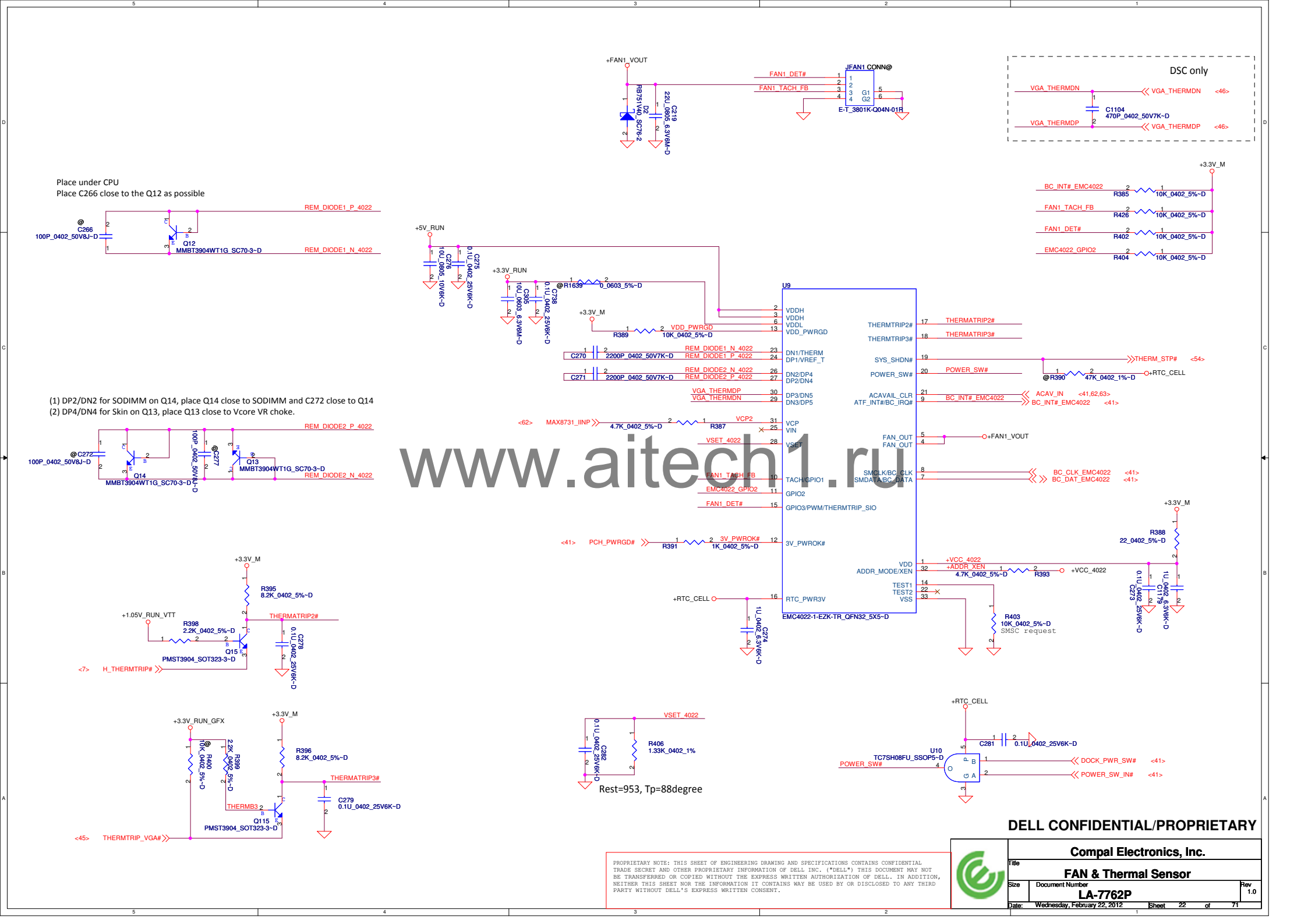
Place under CPU
Place C266 close to the Q12 as possible
(1) DP2/DN2 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
(2) DP4/DN4 for Skin on Q13, place Q13 close to Vcore VR choke.
DSC only
Rest=953, Tp=88degree
SMSC request
U9
EMC4022-1-EZK-TR_QFN32_5X5~D
JFAN1 CONN@
E-T_3801K-Q04N-01R
Q12 MMBT3904WT1G_SC70-3~D
Q13 MMBT3904WT1G_SC70-3~D
Q14 MMBT3904WT1G_SC70-3~D
Q15 PMST3904_SOT323-3~D
Q115 PMST3904_SOT323-3~D
U10 TC7SH08FU_SSOP5~D
D2 RB751V40_SC76-2
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FAN & Thermal Sensor
Document Number
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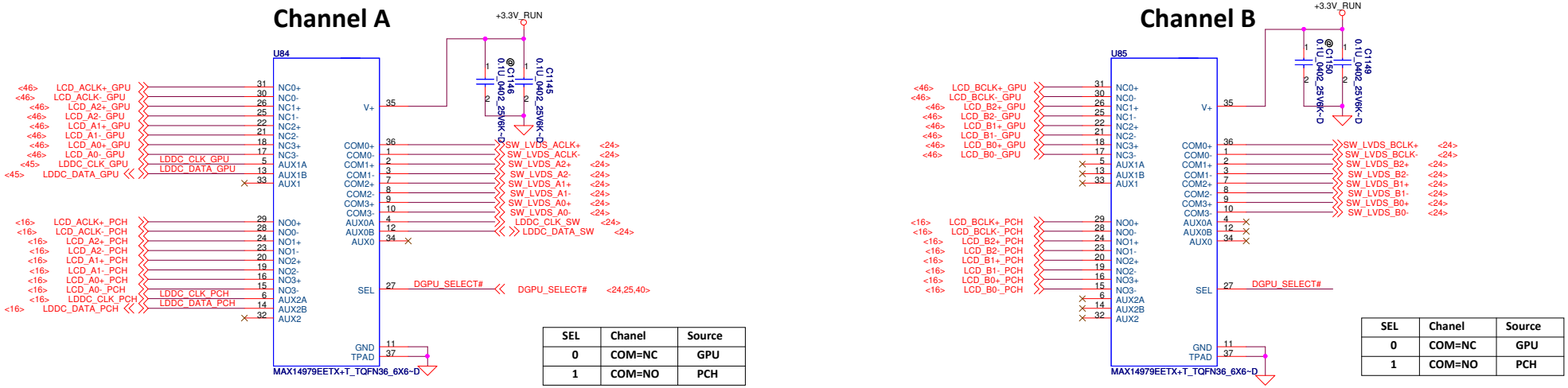
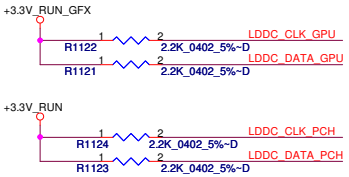


SEL	Chanel	Source
0	COM=NC	GPU
1	COM=NO	PCH

SEL	Chanel	Source
0	COM=NC	GPU
1	COM=NO	PCH



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Title: LVDS SW

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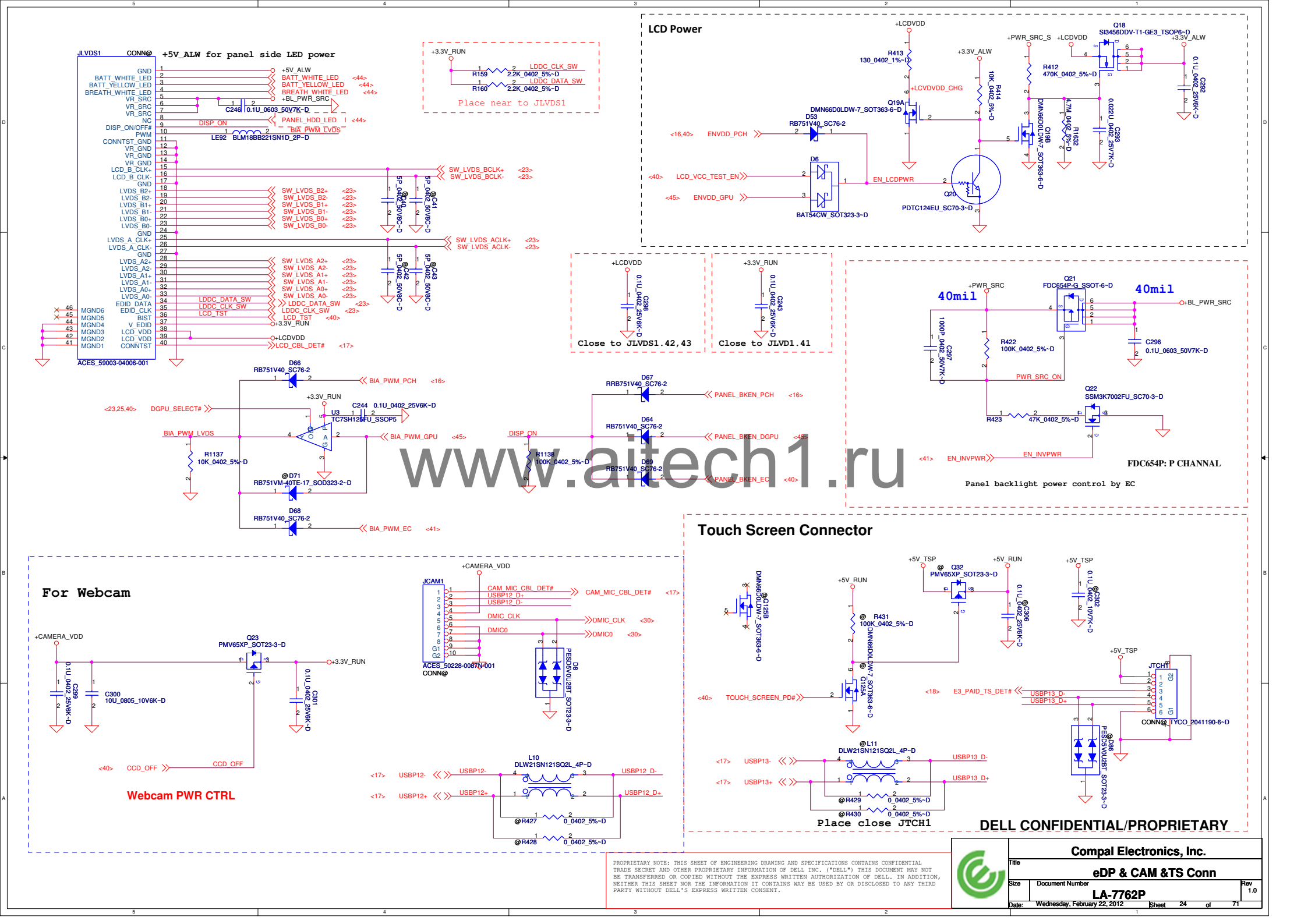
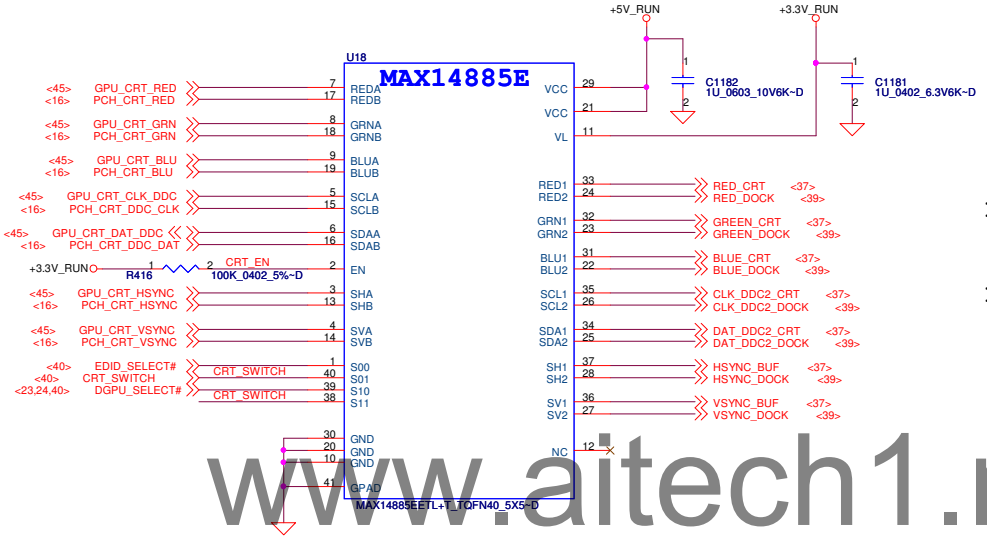


Channel A --> GPU

Channel B --> PCH



Port 1 --> MB Port RGB

Port 2 --> Docking Port RGB

CRT_SWITCH	0	0	1	1
DGPU_SELECT#	0	1	0	1
EDID_SELECT#	0	1	0	1
	A --> Port 1	B --> Port 1	A --> Port 2	B --> Port 2

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Compal Electronics, Inc.

Title: CRT/Video switch

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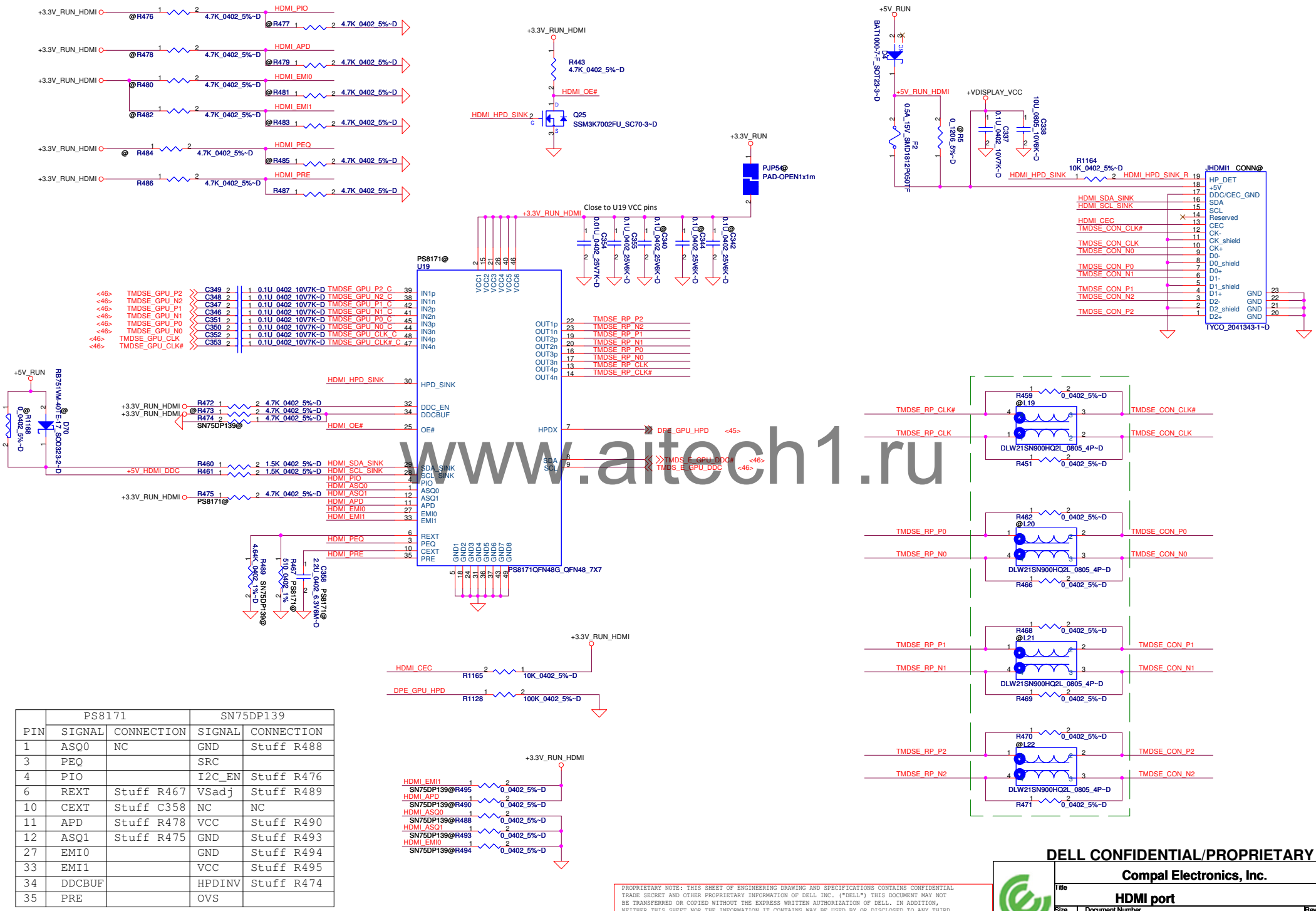

PS8171			SN75DP139	
PIN	SIGNAL	CONNECTION	SIGNAL	CONNECTION
1	ASQ0	NC	GND	Stuff R488
3	PEQ		SRC	
4	PIO		I2C_EN	Stuff R476
6	REXT	Stuff R467	VSadj	Stuff R489
10	CEXT	Stuff C358	NC	NC
11	APD	Stuff R478	VCC	Stuff R490
12	ASQ1	Stuff R475	GND	Stuff R493
27	EMI0		GND	Stuff R494
33	EMI1		VCC	Stuff R495
34	DDCBUF		HPDINV	Stuff R474
35	PRE		OVS	

Compal Electronics, Inc.

Title: HDMI port

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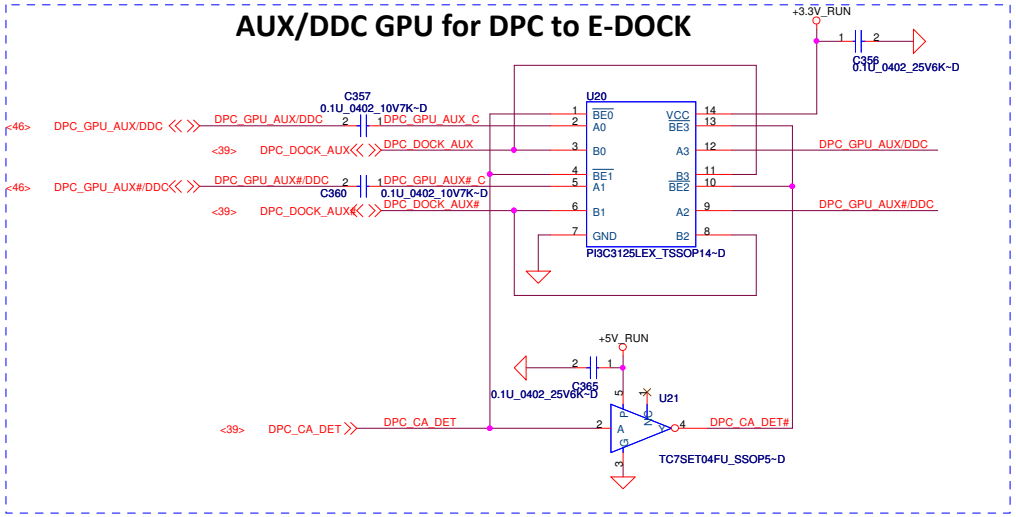
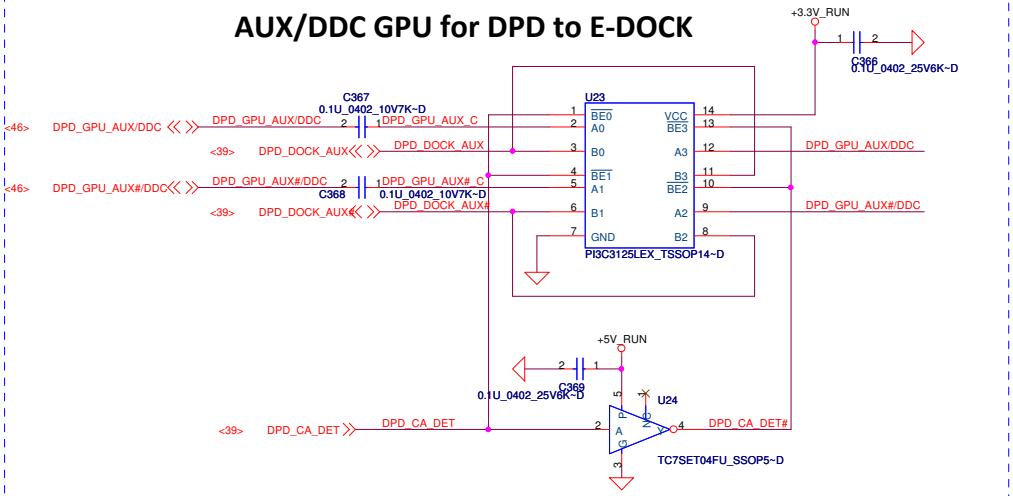
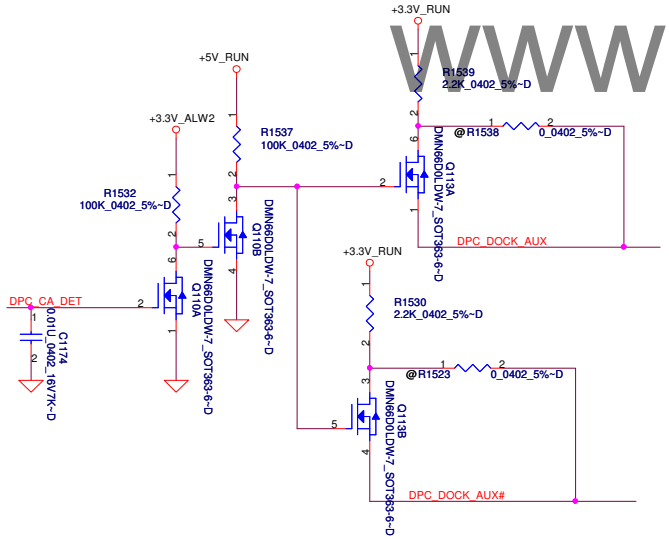
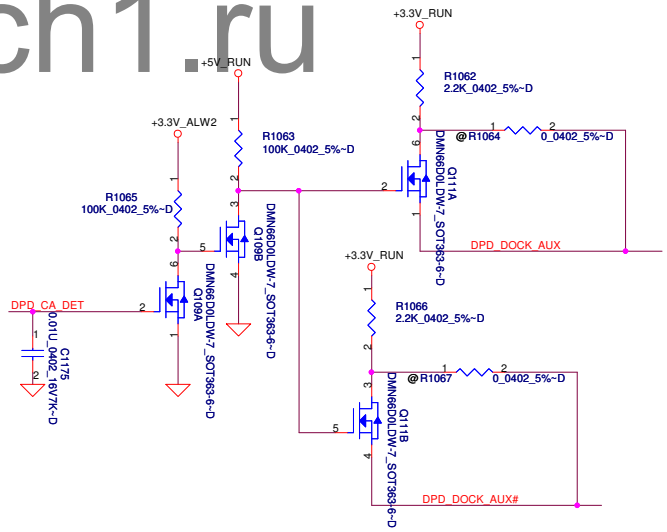
AUX/DDC GPU for DPC to E-DOCK

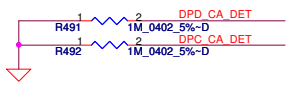


AUX/DDC GPU for DPD to E-DOCK









Compal Electronics, Inc.	
Title	DP AUX SW
Size	Document Number: LA-7762P
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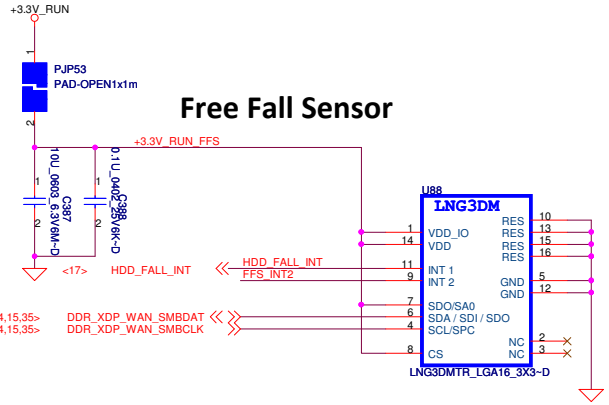

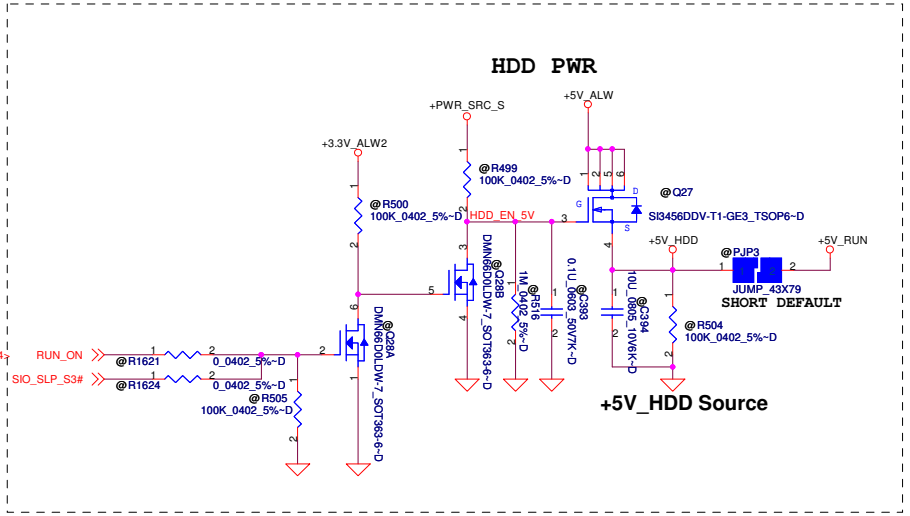

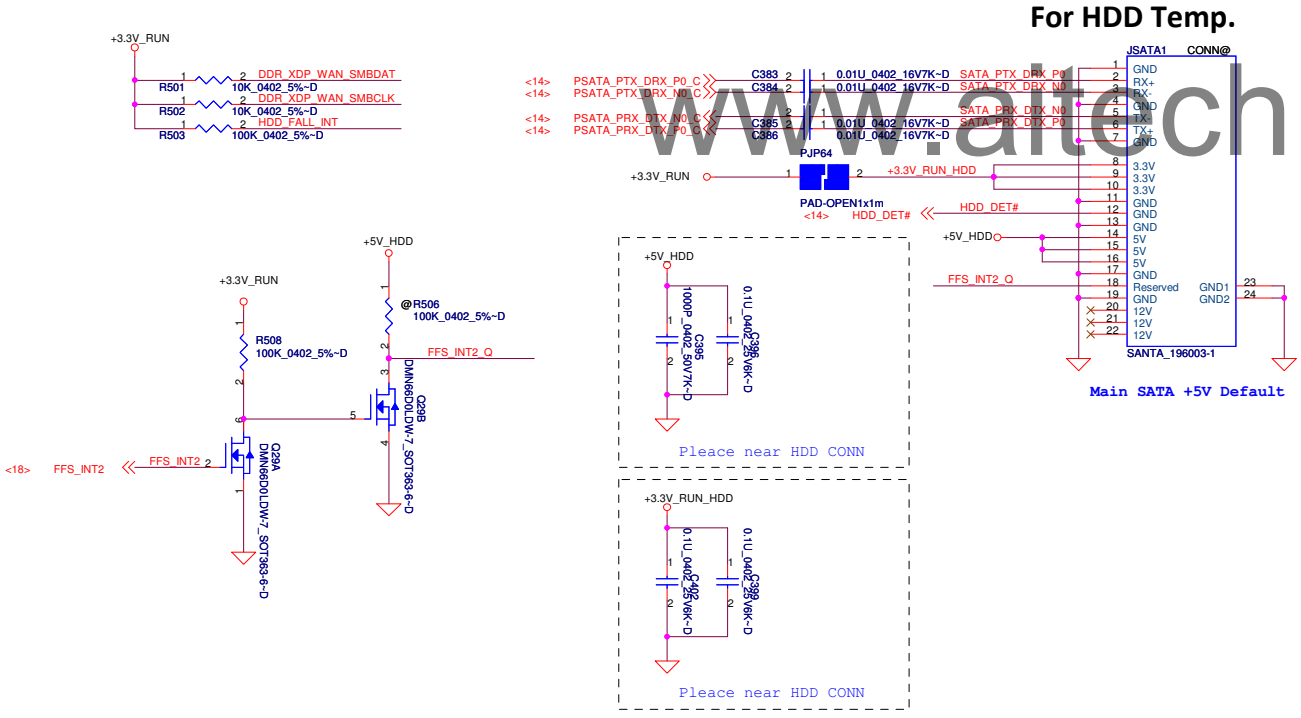

Compal Electronics, Inc.

Title: HDD CONNECTOR

Size | Document Number: LA-7762P | Rev: 1.0

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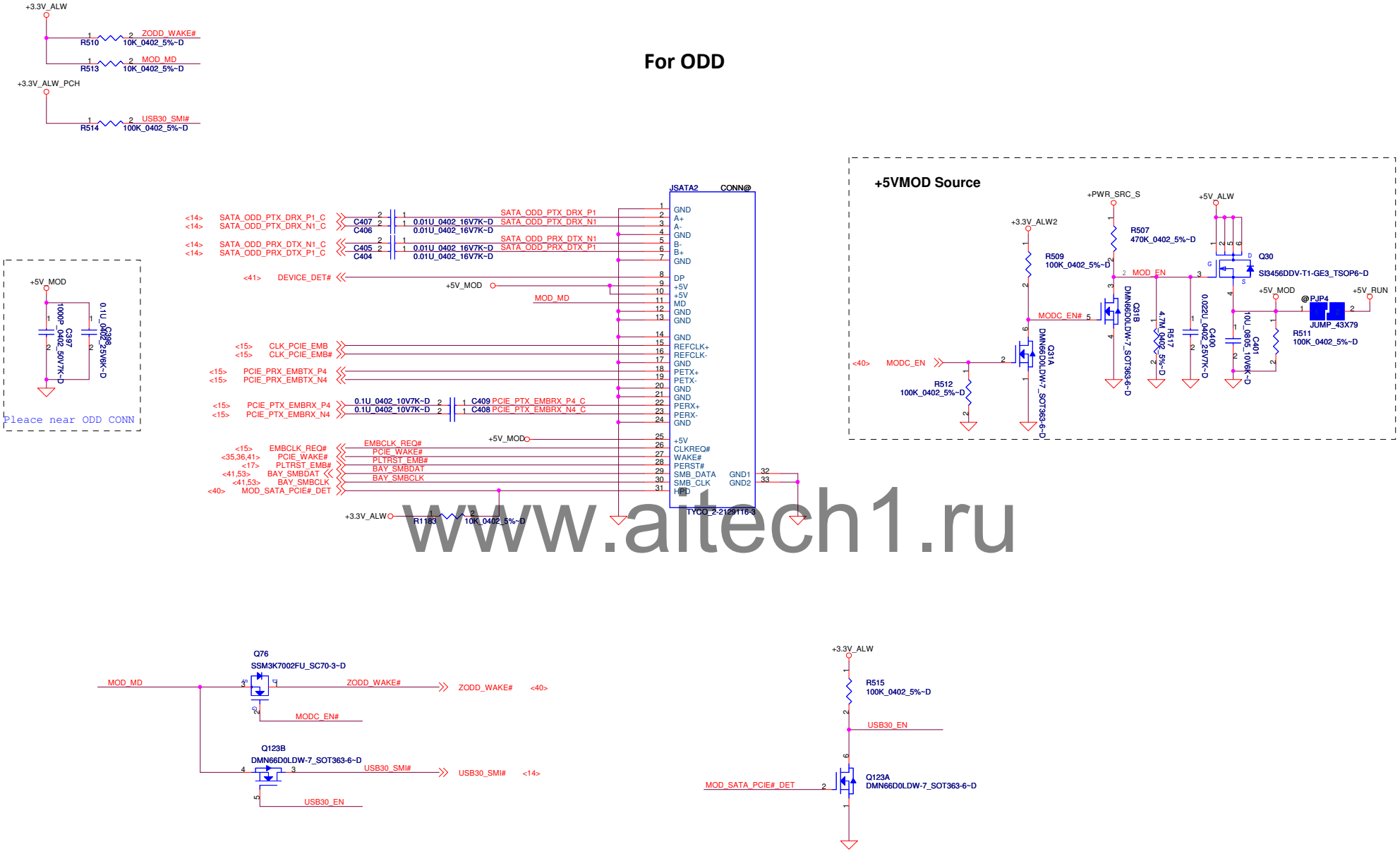
For ODD



Compal Electronics, Inc.

Title: ODD CONNECTOR

Size | Document Number: LA-7762P | Rev: 1.0

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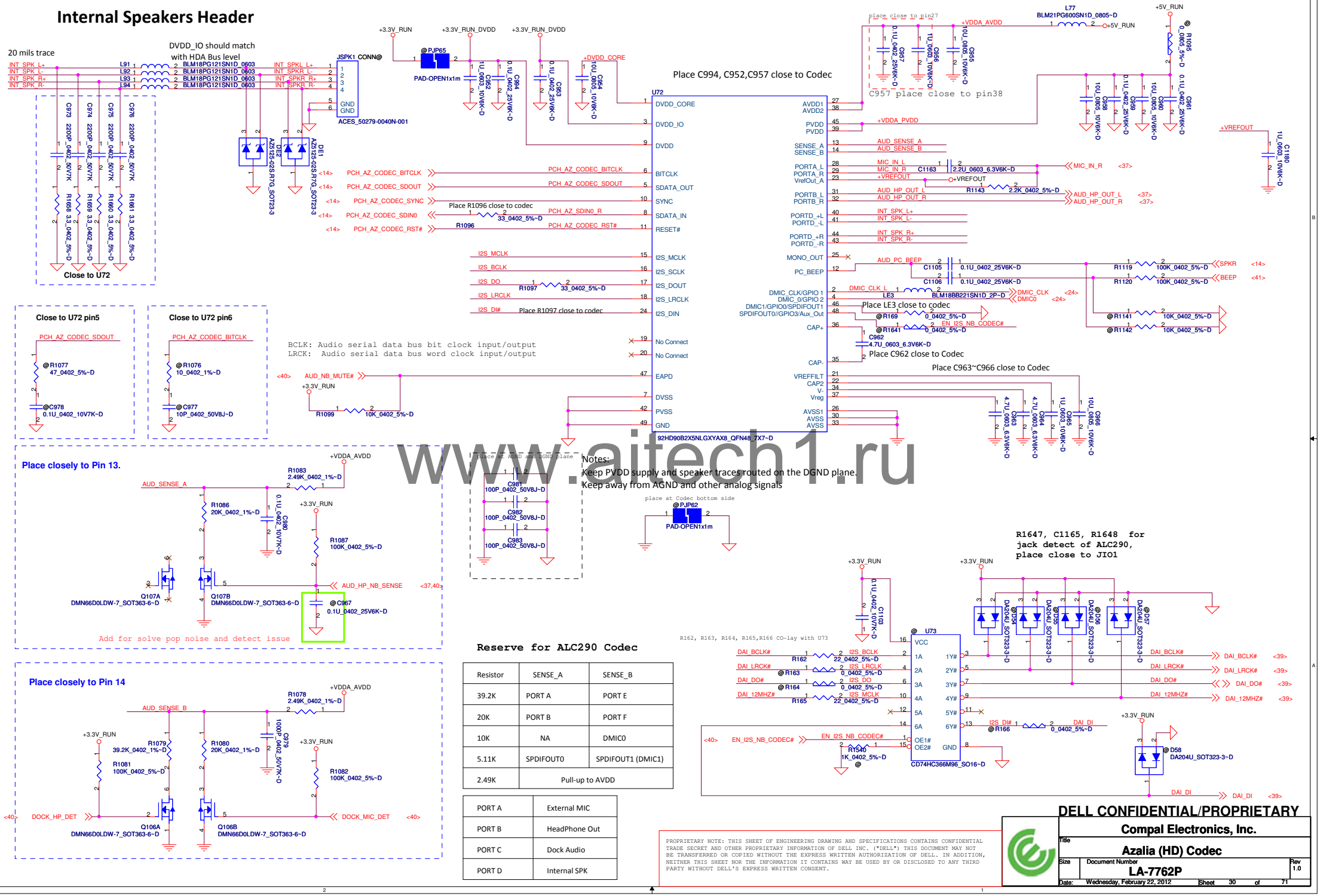
Internal Speakers Header



Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

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Compal Electronics, Inc.

Title: Azalia (HD) Codec

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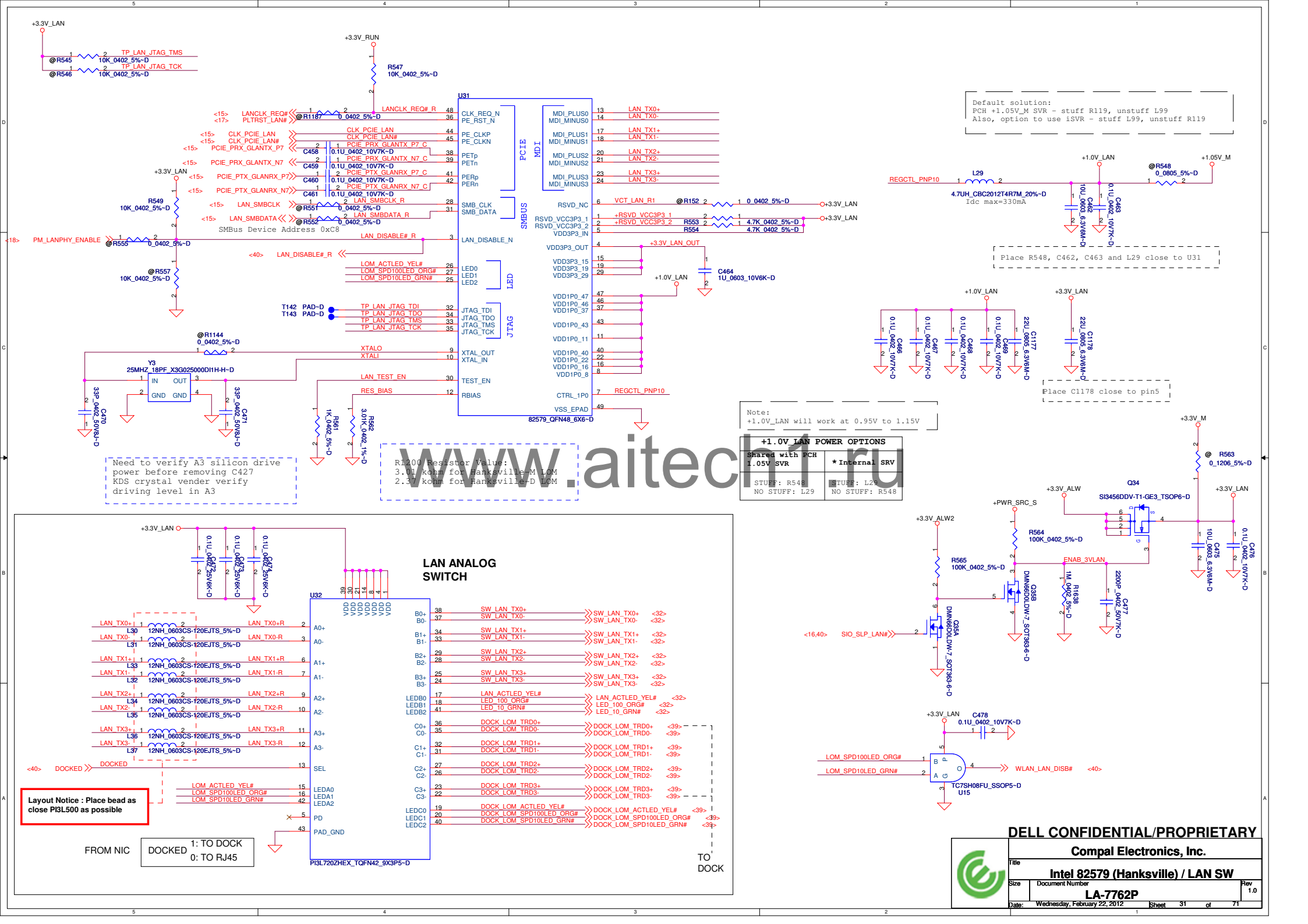

Compal Electronics, Inc.	
Title: Intel 82579 (Hanksville) / LAN SW	
Size	Document Number: LA-7762P
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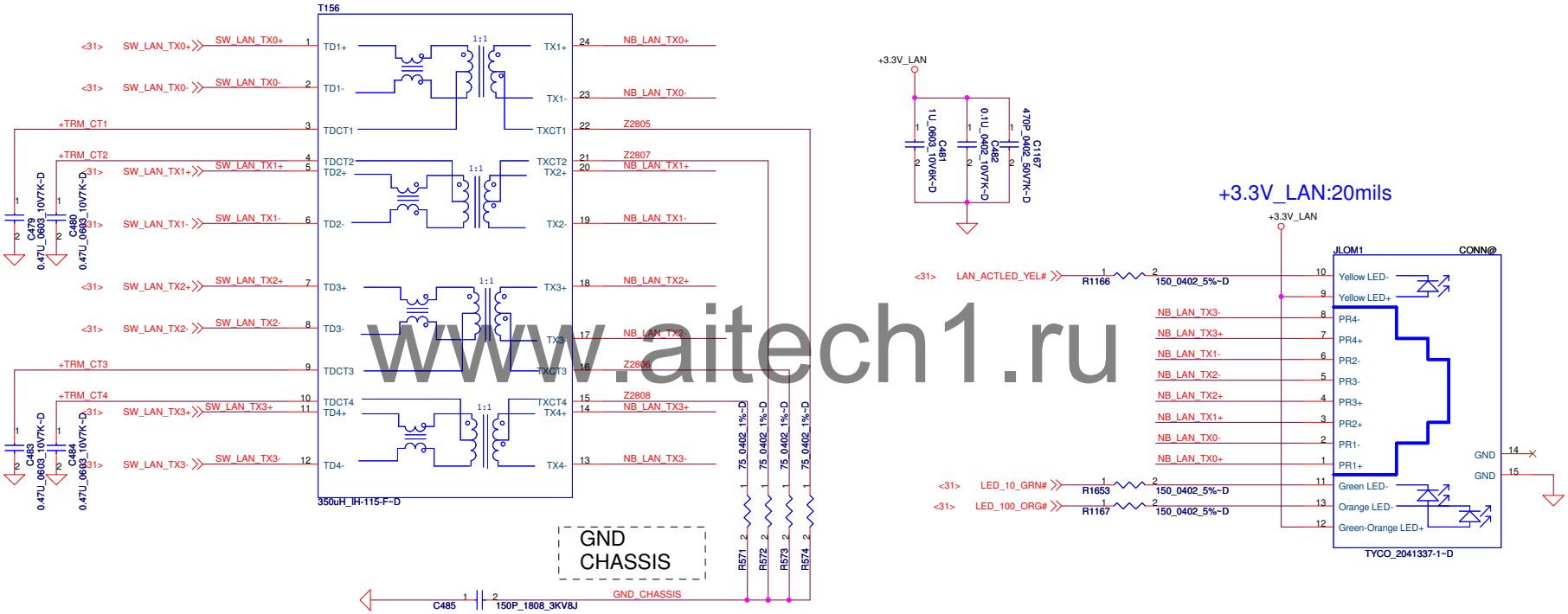

Compal Electronics, Inc.

Title: RJ45 Conn

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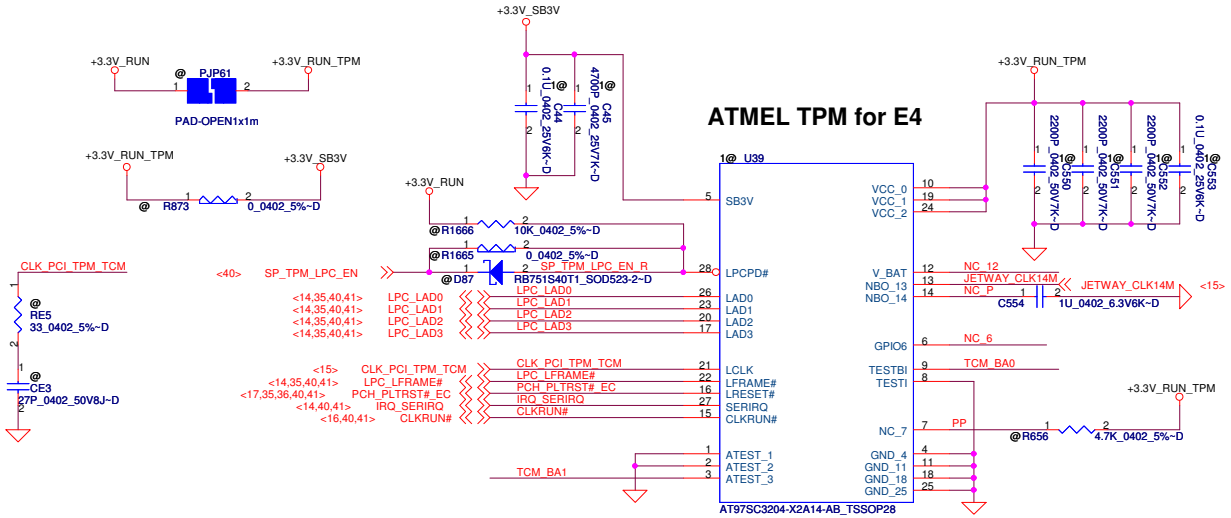
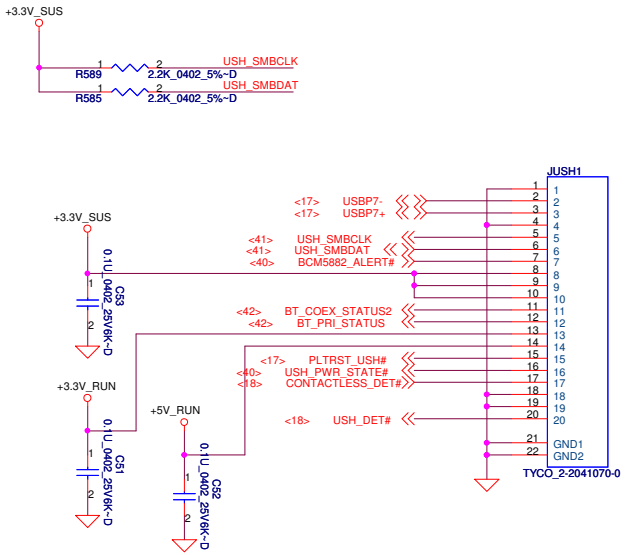
Date: Wednesday, February 22, 2012 | Sheet 32 of 71



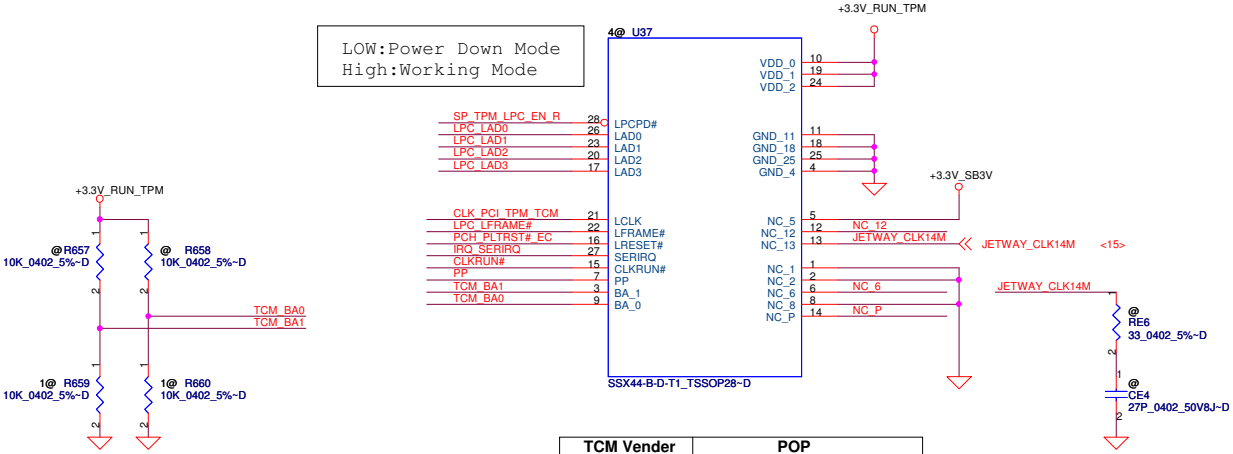


Co-lay U37 and U38

LPC layout: Place TCM first and then end LPC with TPM.

China TCM: NationZ & Jetway co-lay

LOW:Power Down Mode
High:Working Mode



TCM Vender	POP
NationZ	R660, R659, C554, C550
Jetway	C555, RH315

TPM and China TCM Z8H172T Option				
PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 4@	POP	@	@
PCH GPIO39 ->TPM_ID1	PU RH268 PD RH271	@ POP	POP @	POP @
PCH GPIO38 ->TPM_ID0	PU RH267 PD RH270	@ POP	POP @	@ POP

Compal Electronics, Inc.

Title: USH conn/TPM

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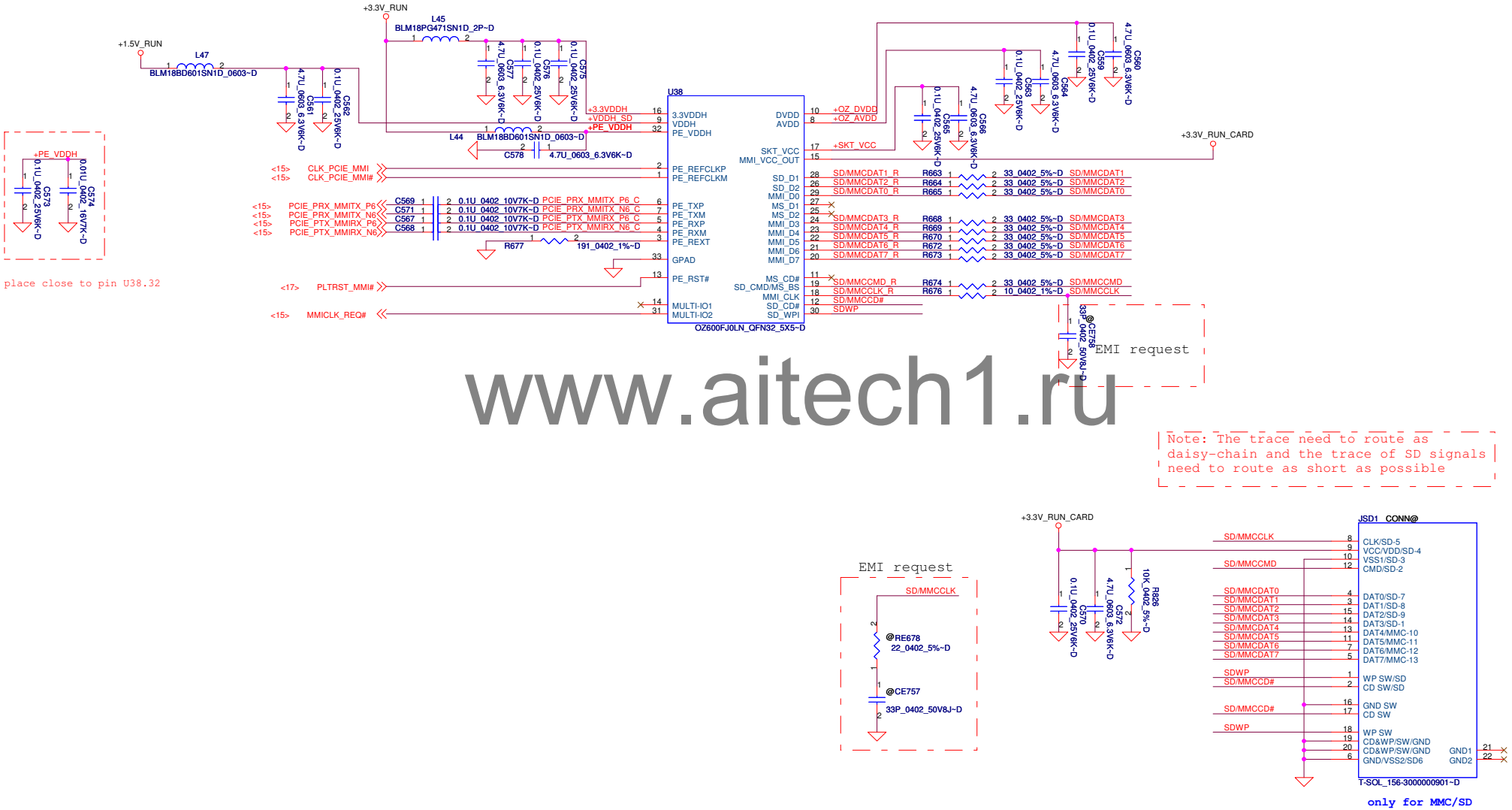

Compal Electronics, Inc.

Title: Card Reader OZ600FJ0

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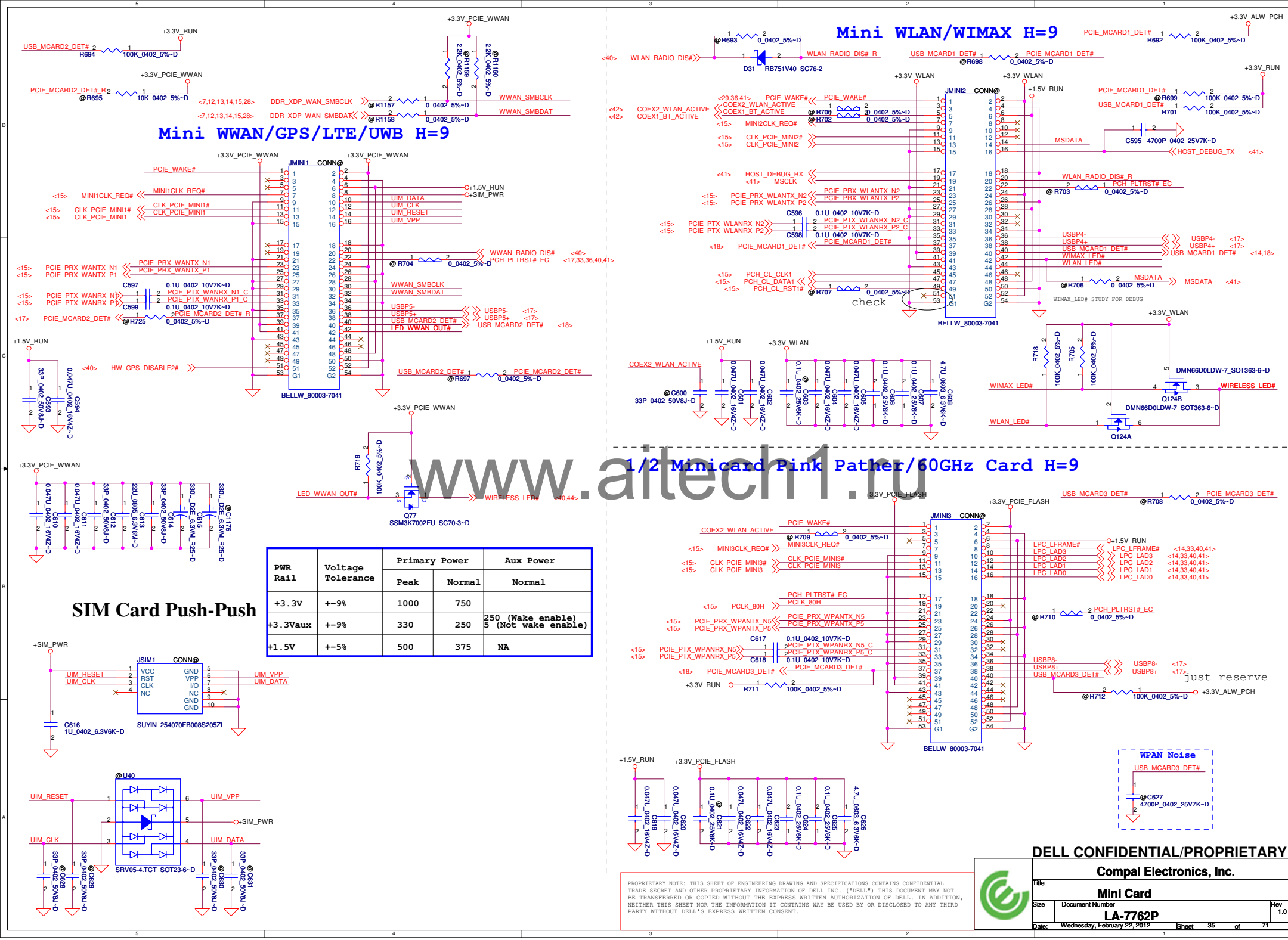

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+-9%	1000	750	
+3.3Vaux	+-9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+-5%	500	375	NA

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Compal Electronics, Inc.

Title: Mini Card

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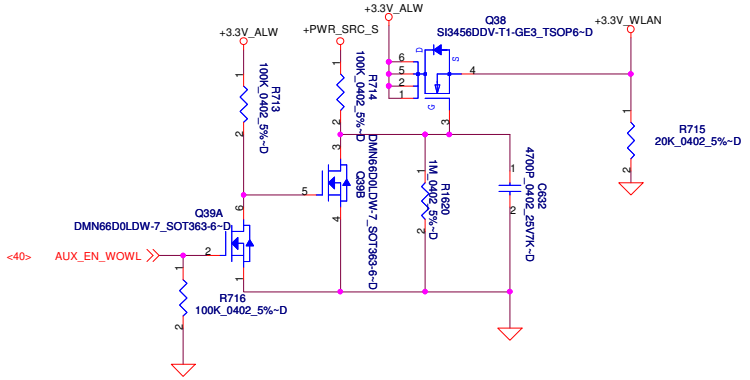
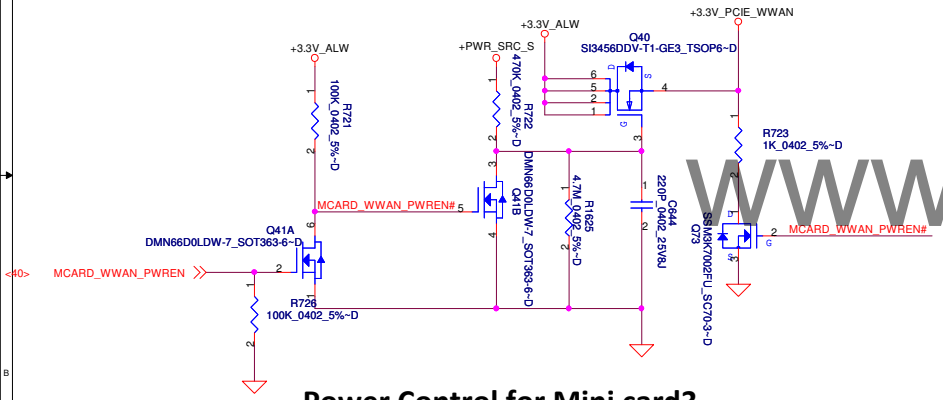
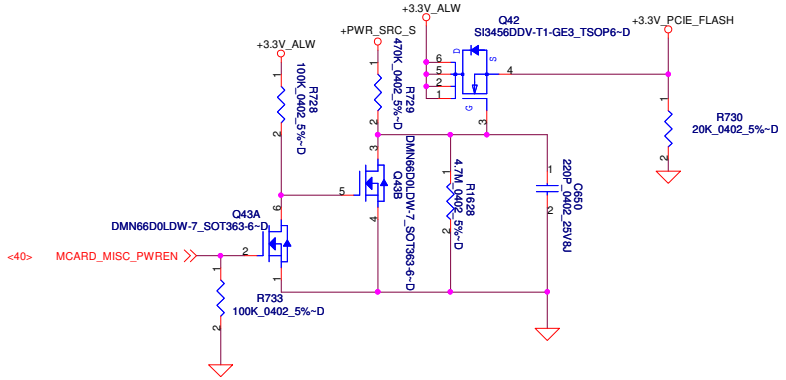
Power Control for Mini card1



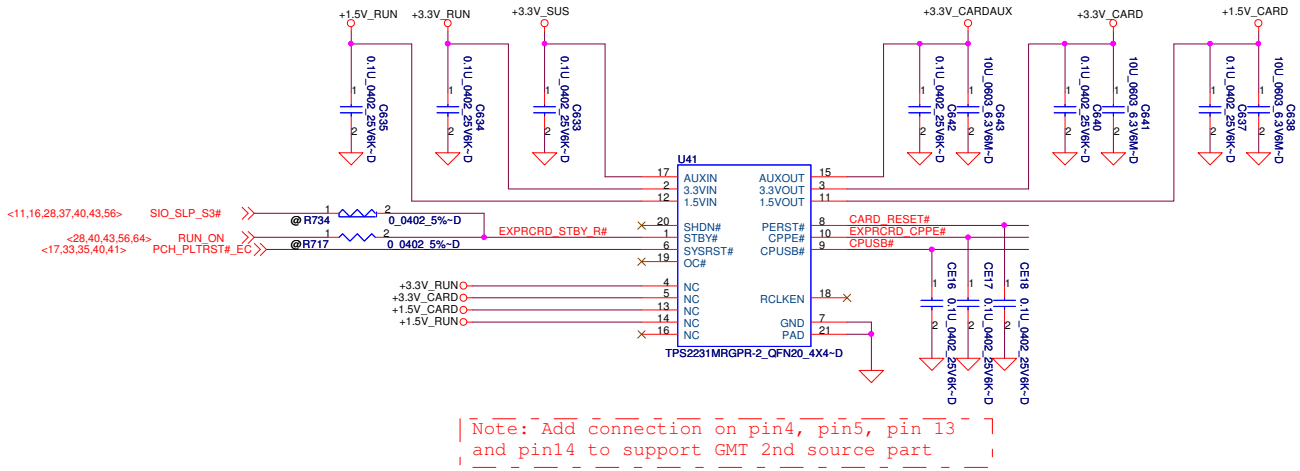
Power Control for Mini card2



Power Control for Mini card3

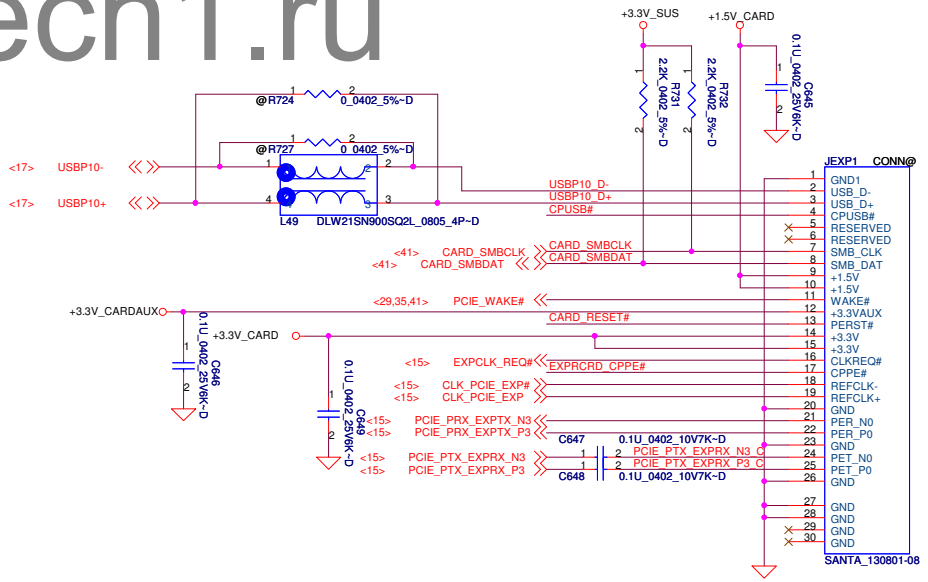


Express Card PWR S/W



Note: Add connection on pin4, pin5, pin 13 and pin14 to support GMT 2nd source part

Express Card Conn.



Compal Electronics, Inc.

Title: PCIE-SATA SW / PCIE PWR

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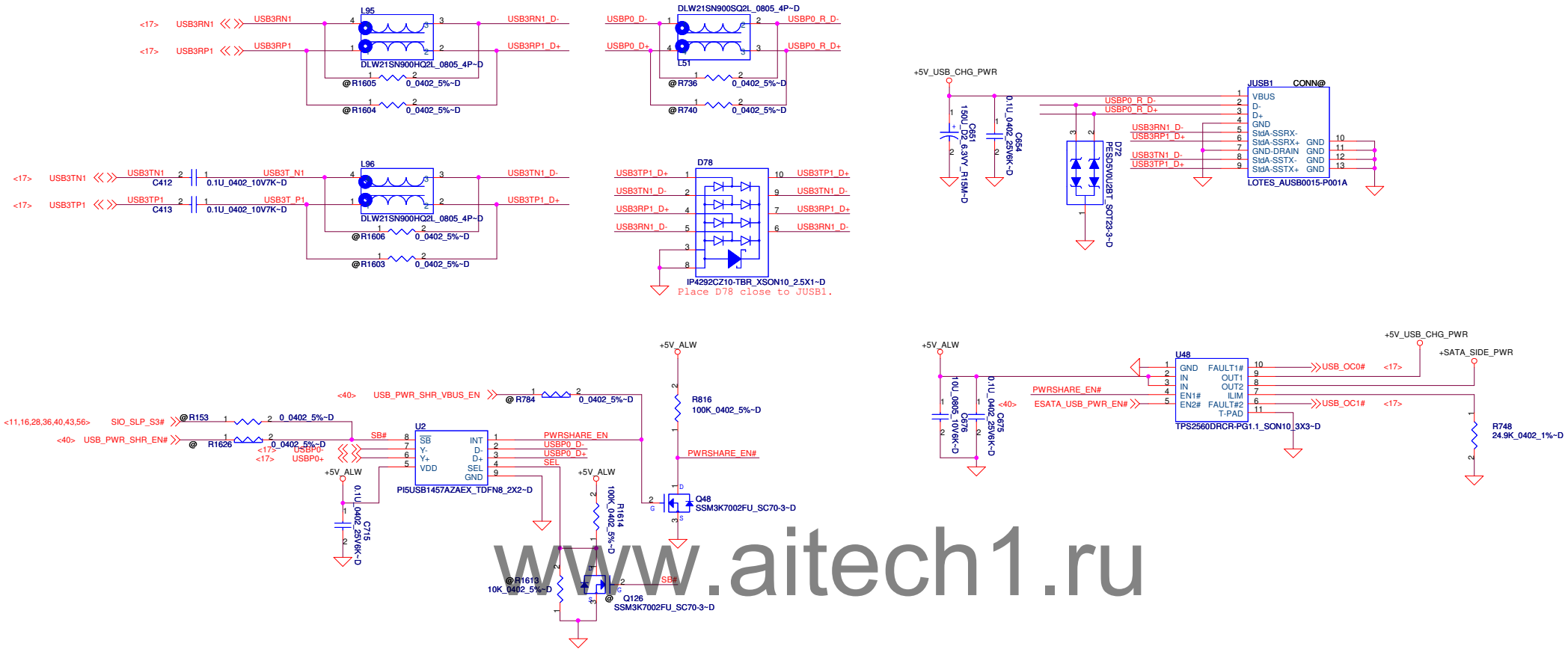
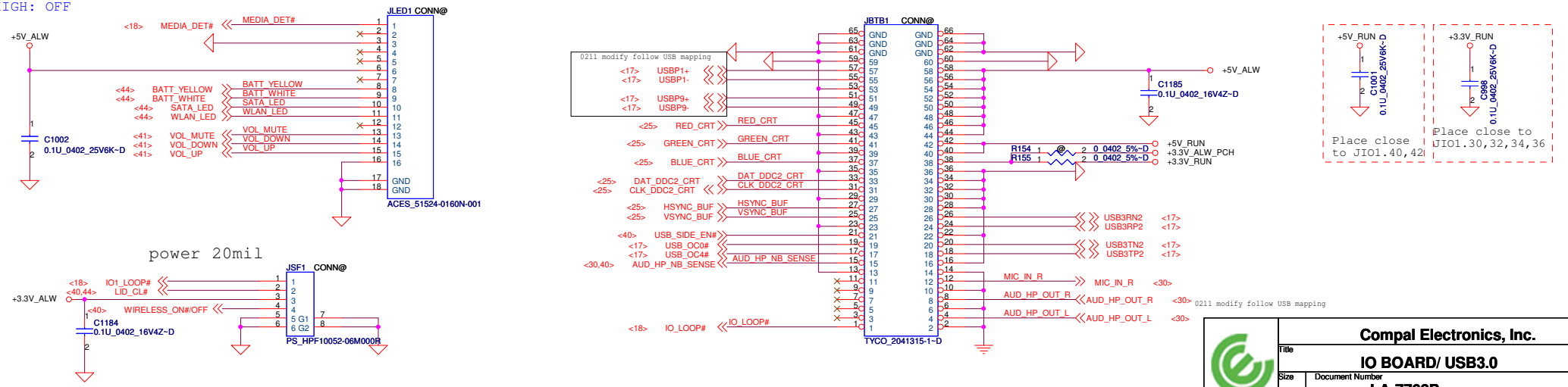


MEDIA BOARD

USBx2 /USB3.0x1 / CRT/ AUDIO JACK IO BOARD

Defult on,
WIRELESS_ON/OFF#:
LOW: ON
HIGH: OFF



normal trace 50ohm

Compal Electronics, Inc.	
Title	IO BOARD/ USB3.0
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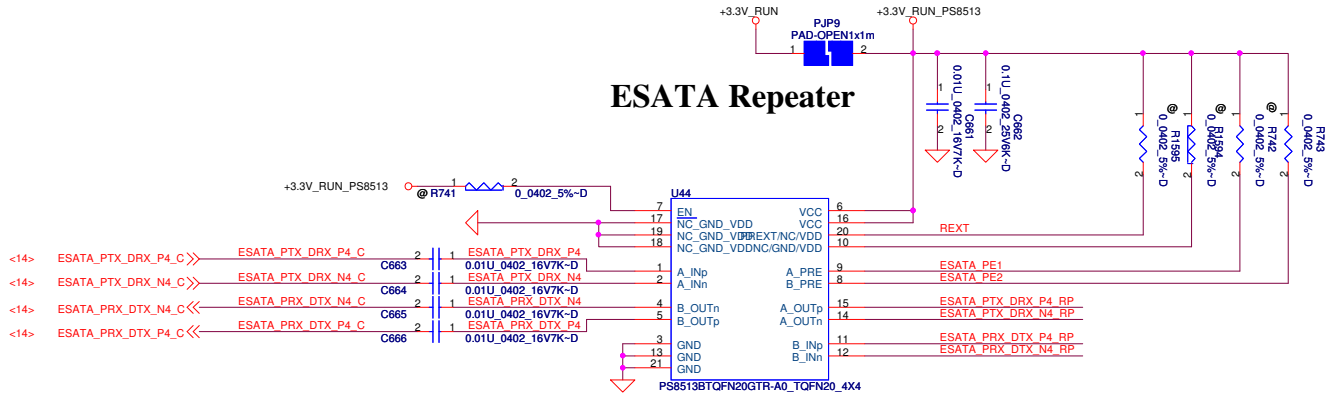
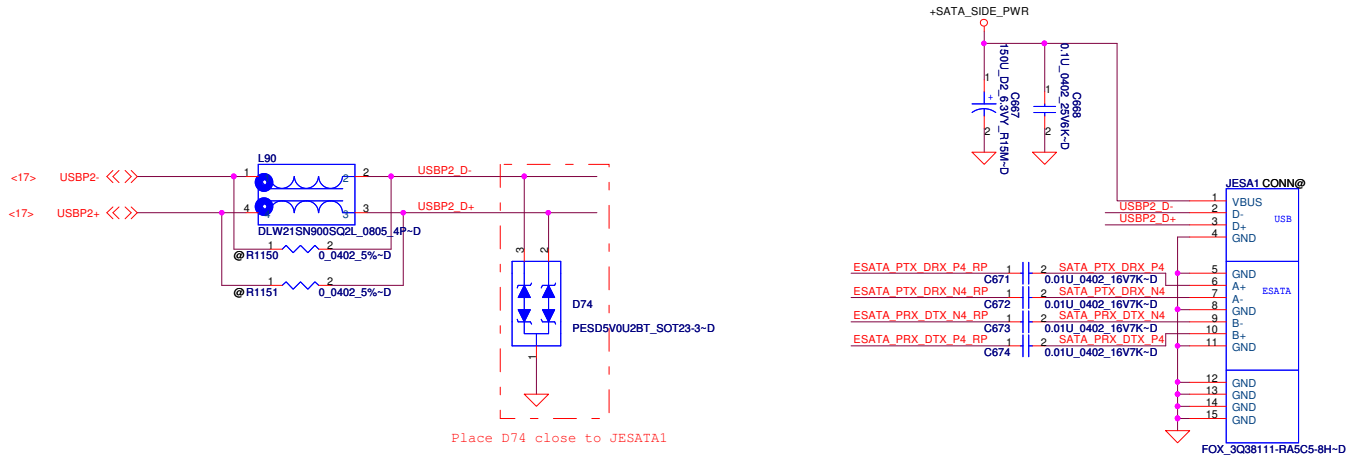


Note: +ESATA_DEW1, +ESATA_DEW2, +ESATA_EQ1, +ESATA_EQ2 need to route 10 mils and R1584~R1587 need to change to 10k and no stuff R1584, R1585 to support TI SN75LVCP601



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Compal Electronics, Inc.	
Title	USB/ESATA/IO/MDC
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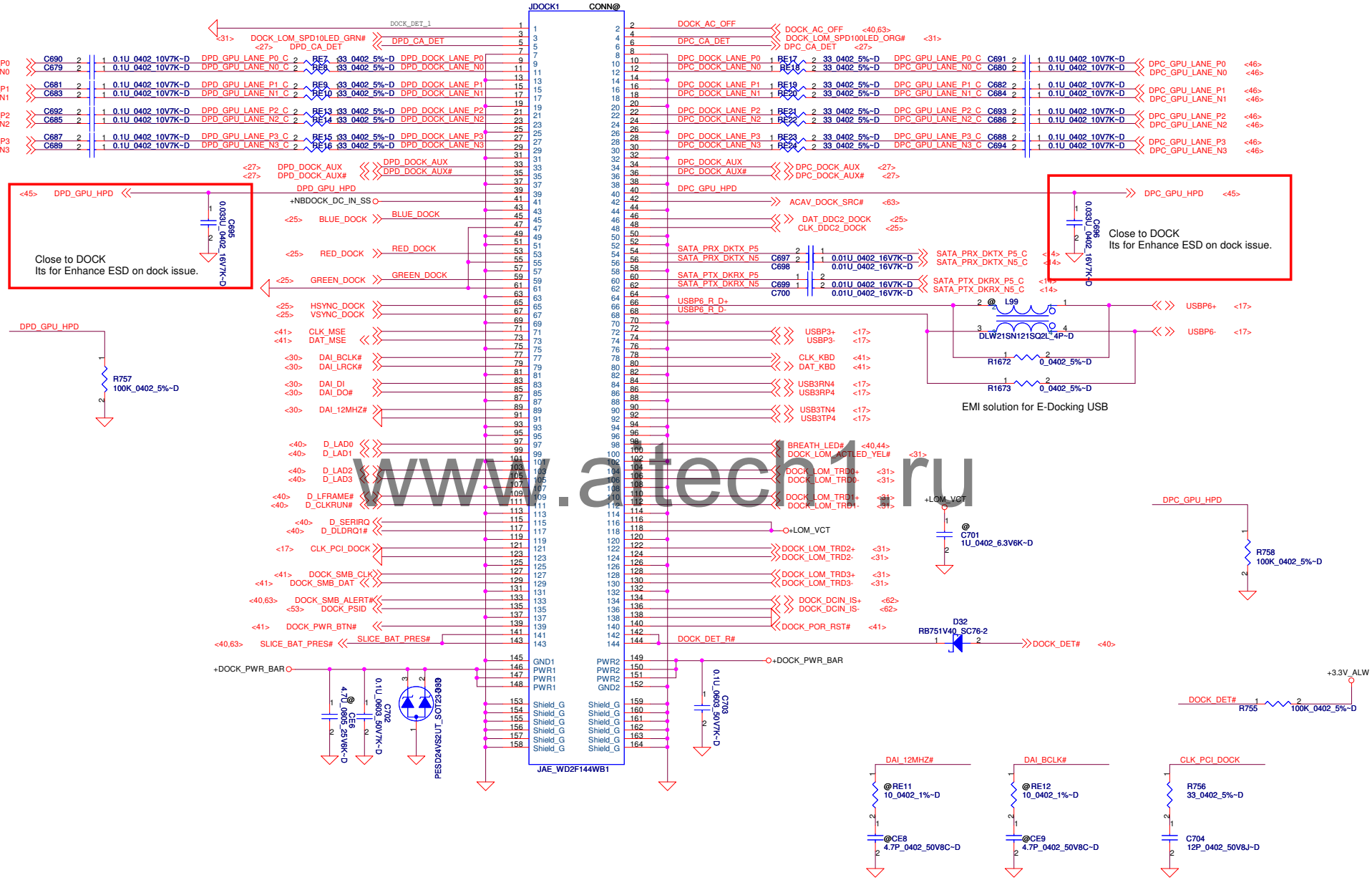

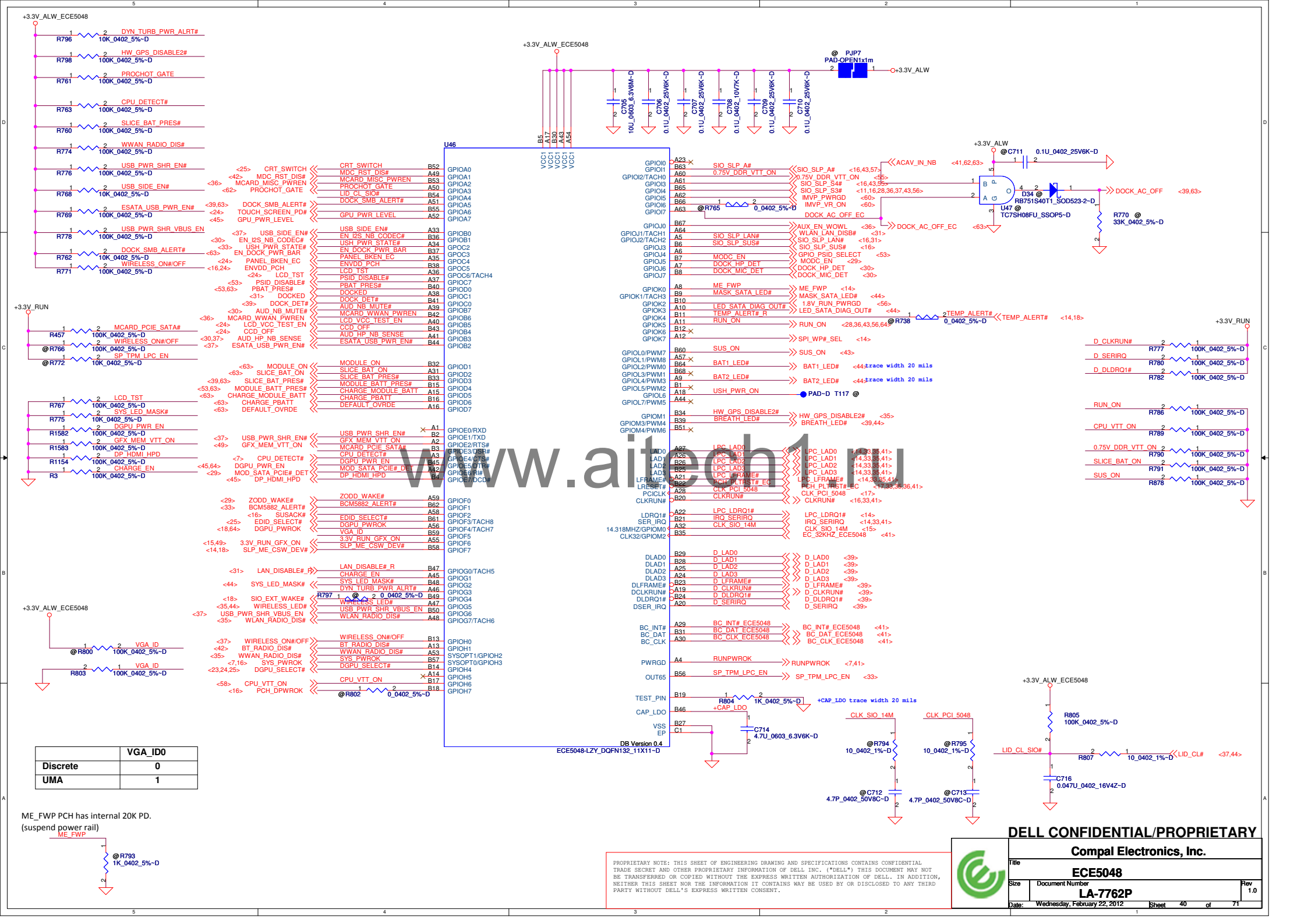

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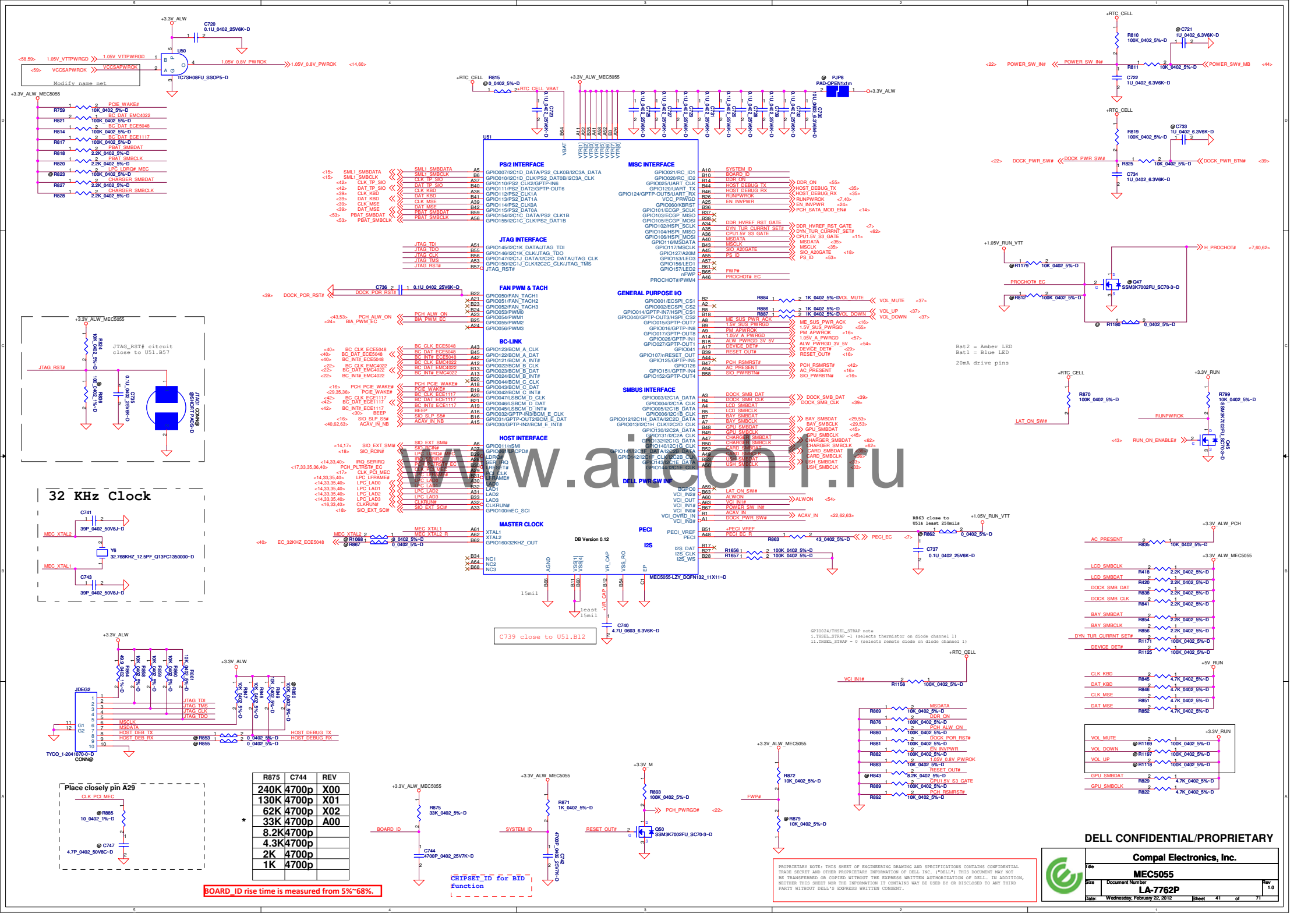
Compal Electronics, Inc.

Title: ECE5048

Size | Document Number: LA-7762P | Rev: 1.0

Date: Wednesday, February 22, 2012 | Sheet 40 of 71



R875	C744	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	A00
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

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Compal Electronics, Inc.	
Title	MEC5055
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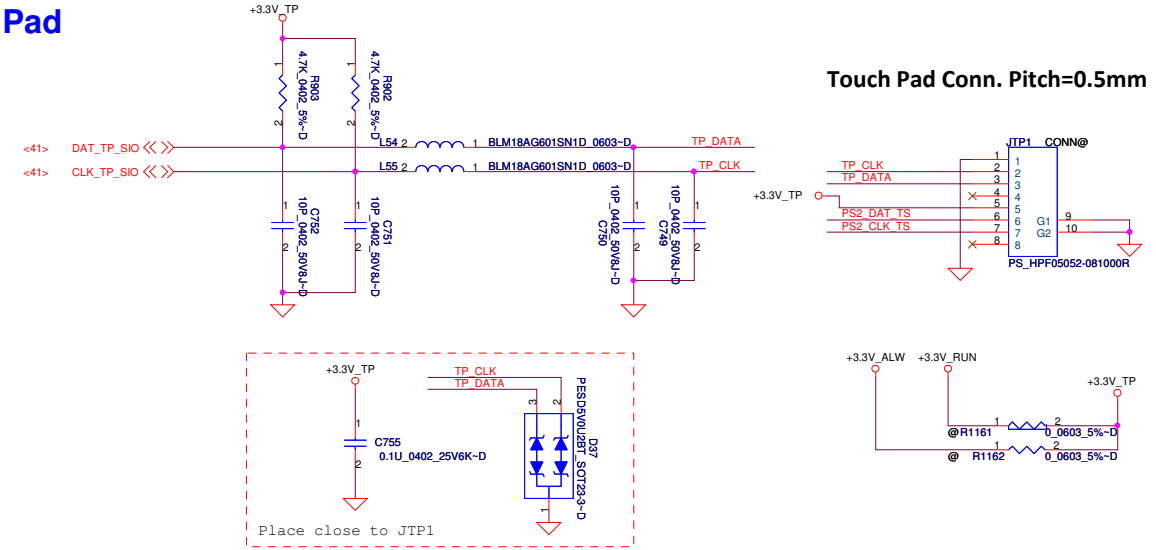
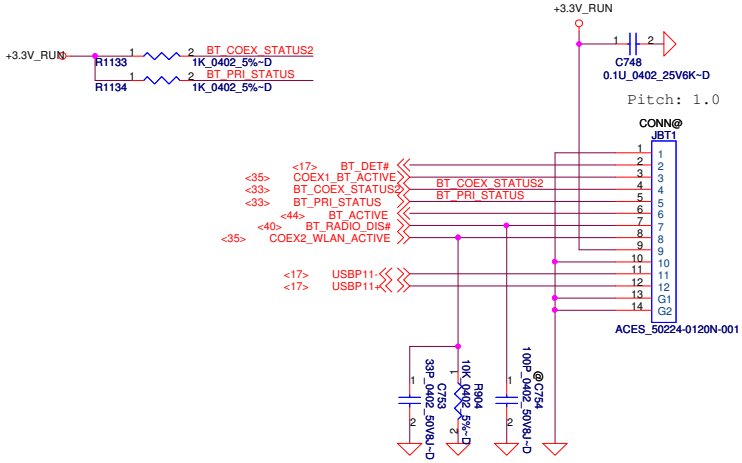
Touch Pad

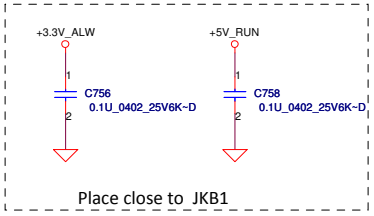


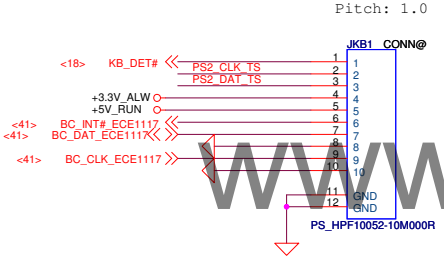
Touch Pad Conn. Pitch=0.5mm

BlueTooth



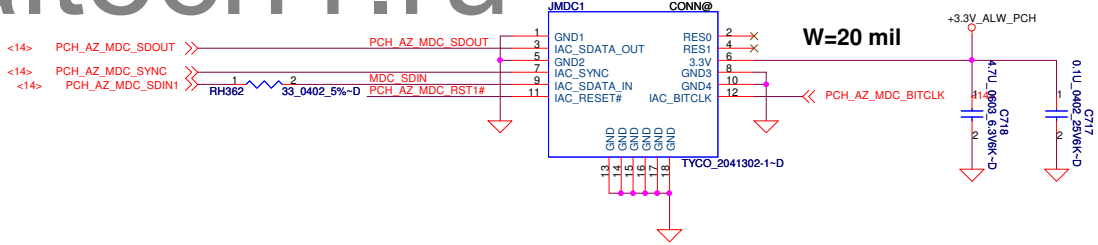
Keyboard

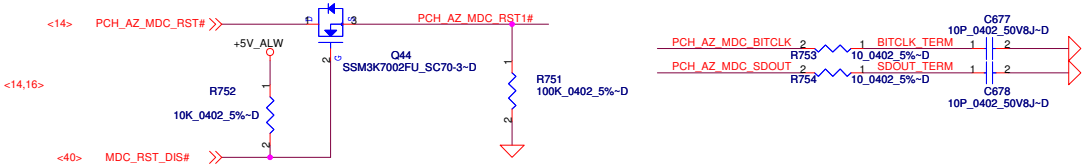




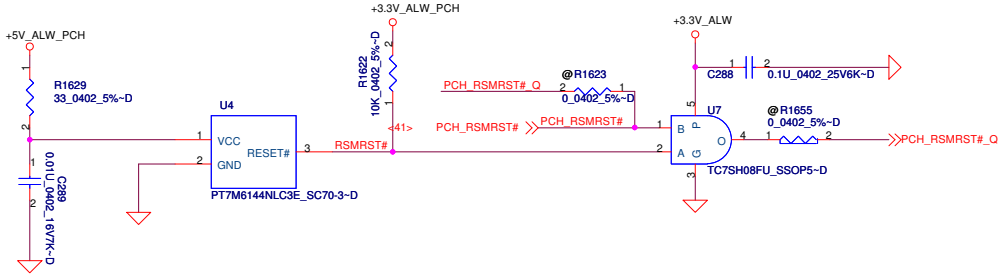
MDC

MDC CONN. H=5.5, Pitch=0.8





RSMRST#



Compal Electronics, Inc.

Title: Int KB/TP/BT/RSMRST/MDC

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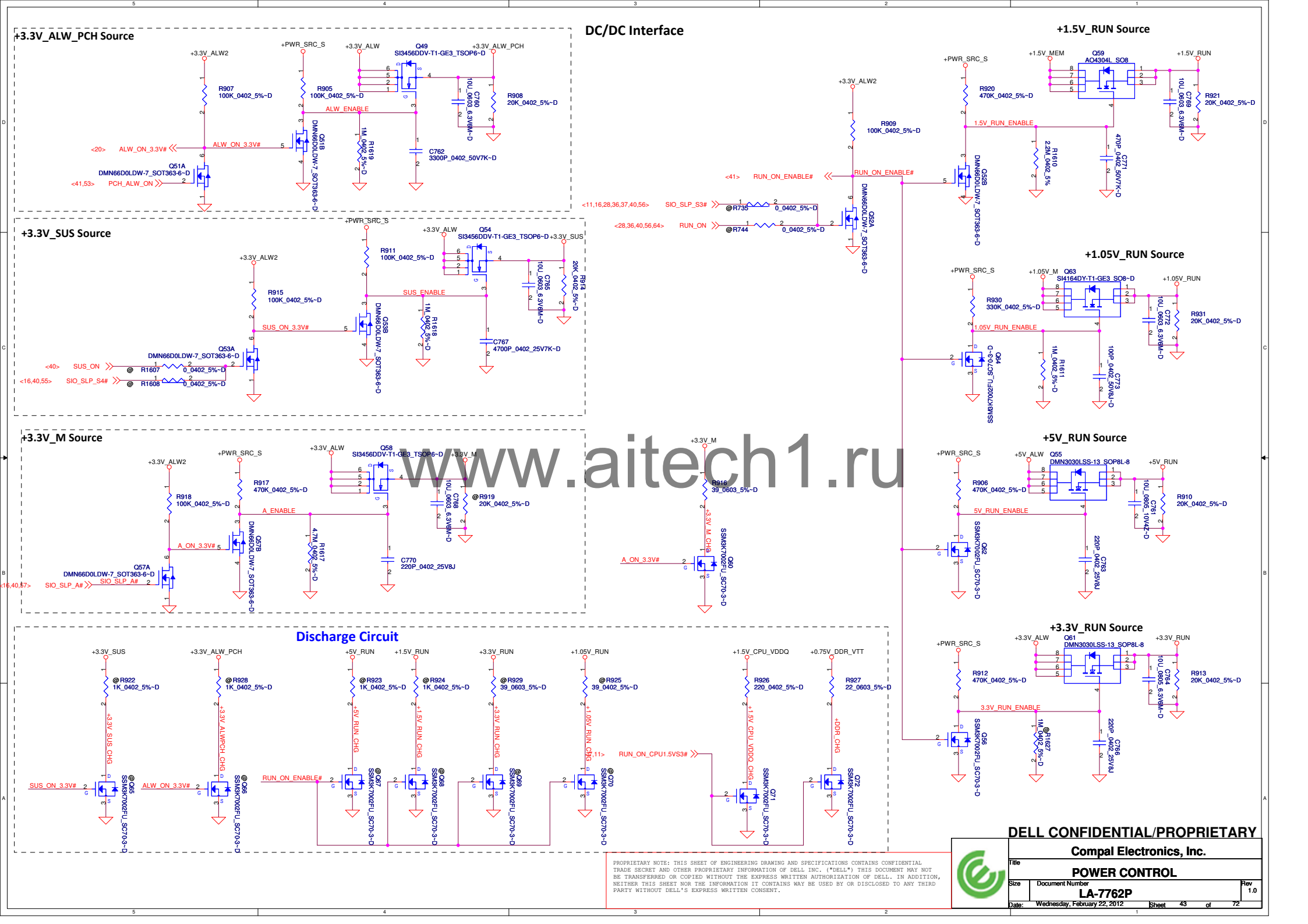
+3.3V_ALW_PCH Source
DC/DC Interface
+1.5V_RUN Source
+3.3V_SUS Source
+1.05V_RUN Source
+3.3V_M Source
+5V_RUN Source
+3.3V_RUN Source
Discharge Circuit
www.aitech1.ru
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Compal Electronics, Inc.
POWER CONTROL
LA-7762P
Wednesday, February 22, 2012
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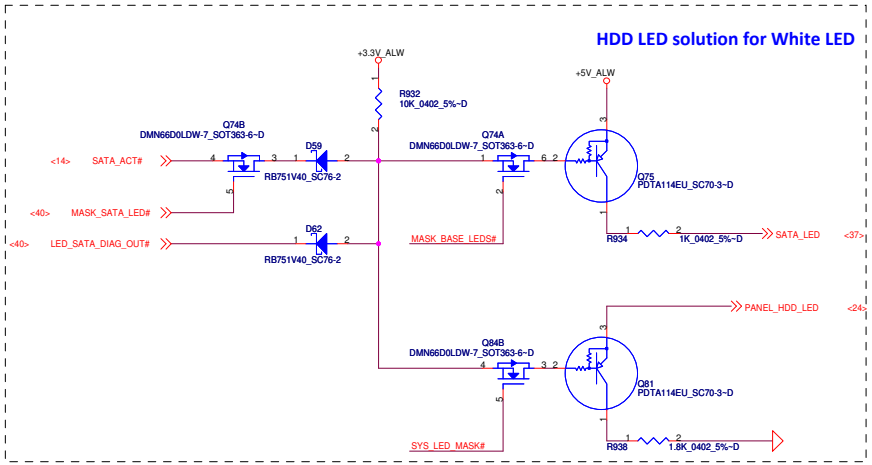
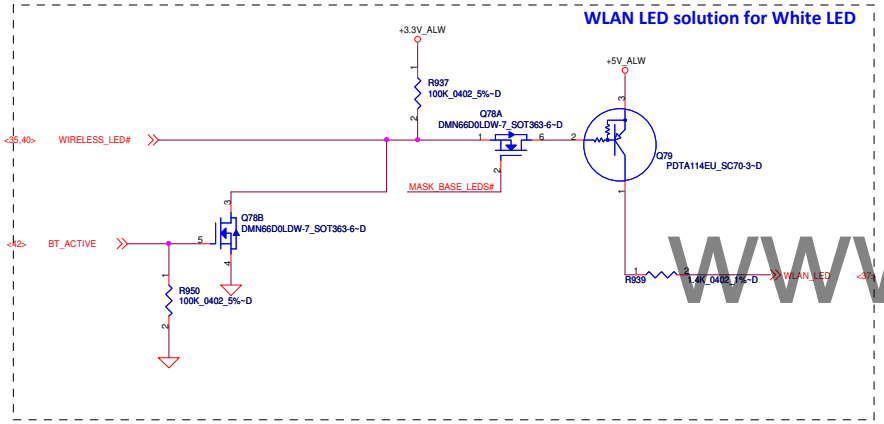
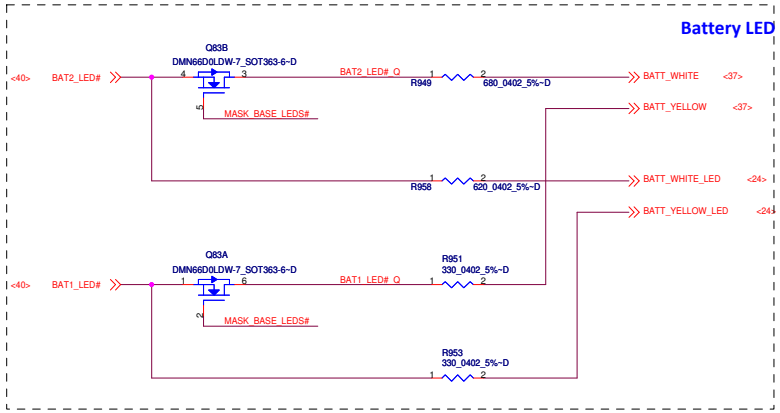
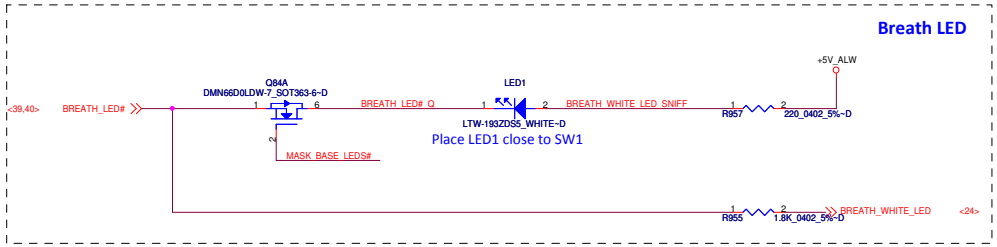
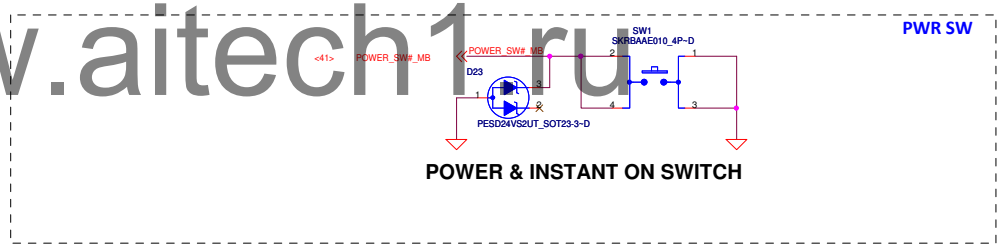


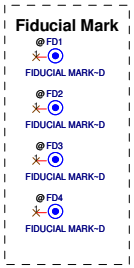


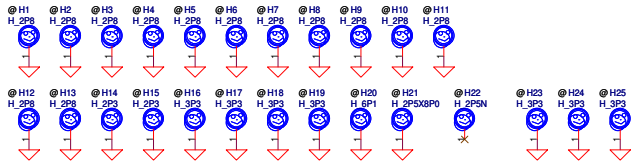


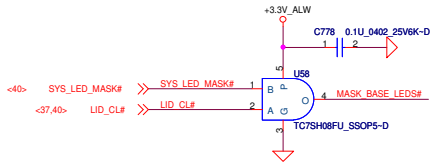


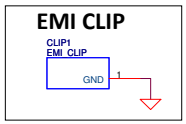


LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1









Compal Electronics, Inc.

Title: PWR SW/LED/PAD/ME

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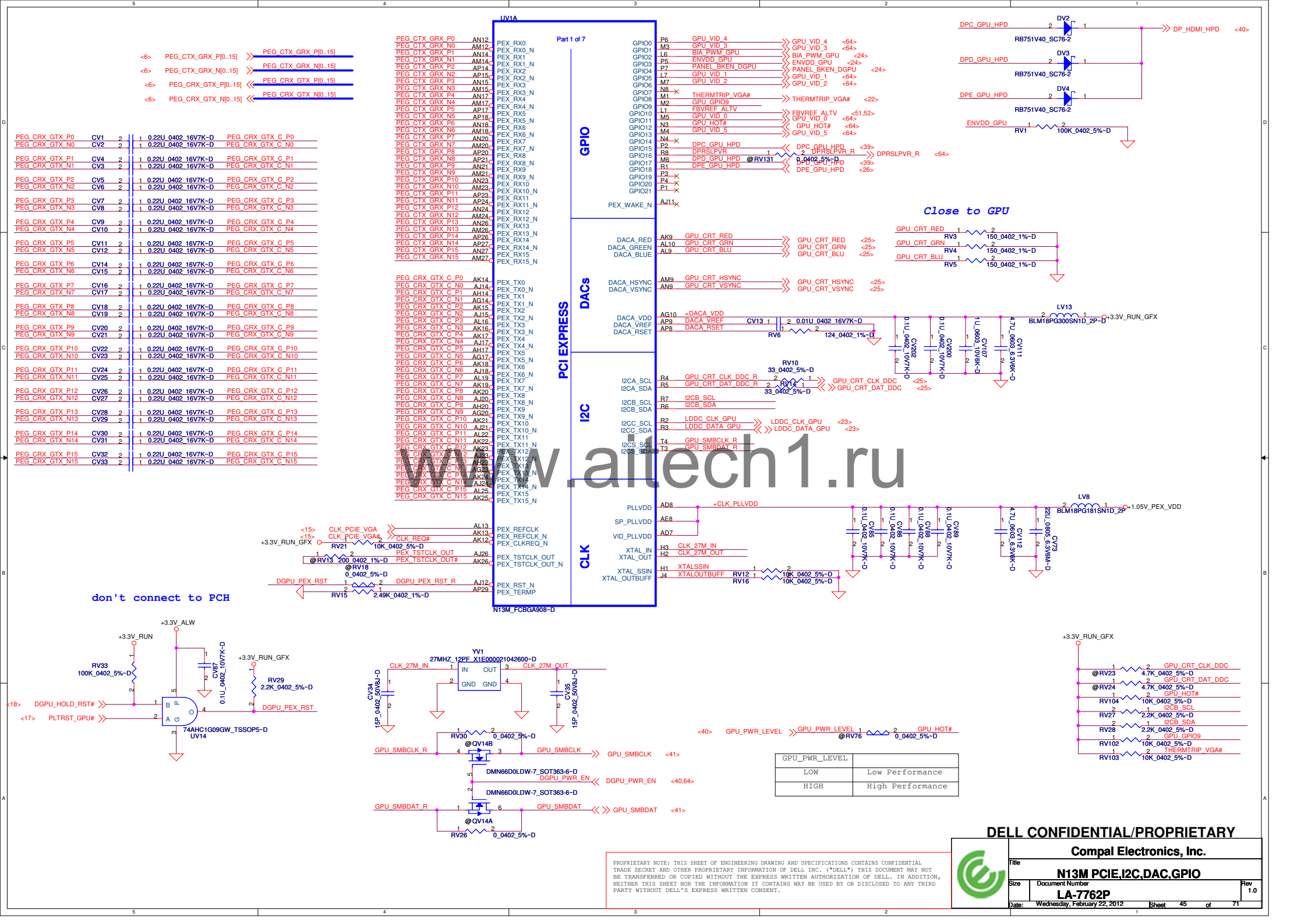

Compal Electronics, Inc.

Title: N13M PCIE,I2C,DAC,GPIO

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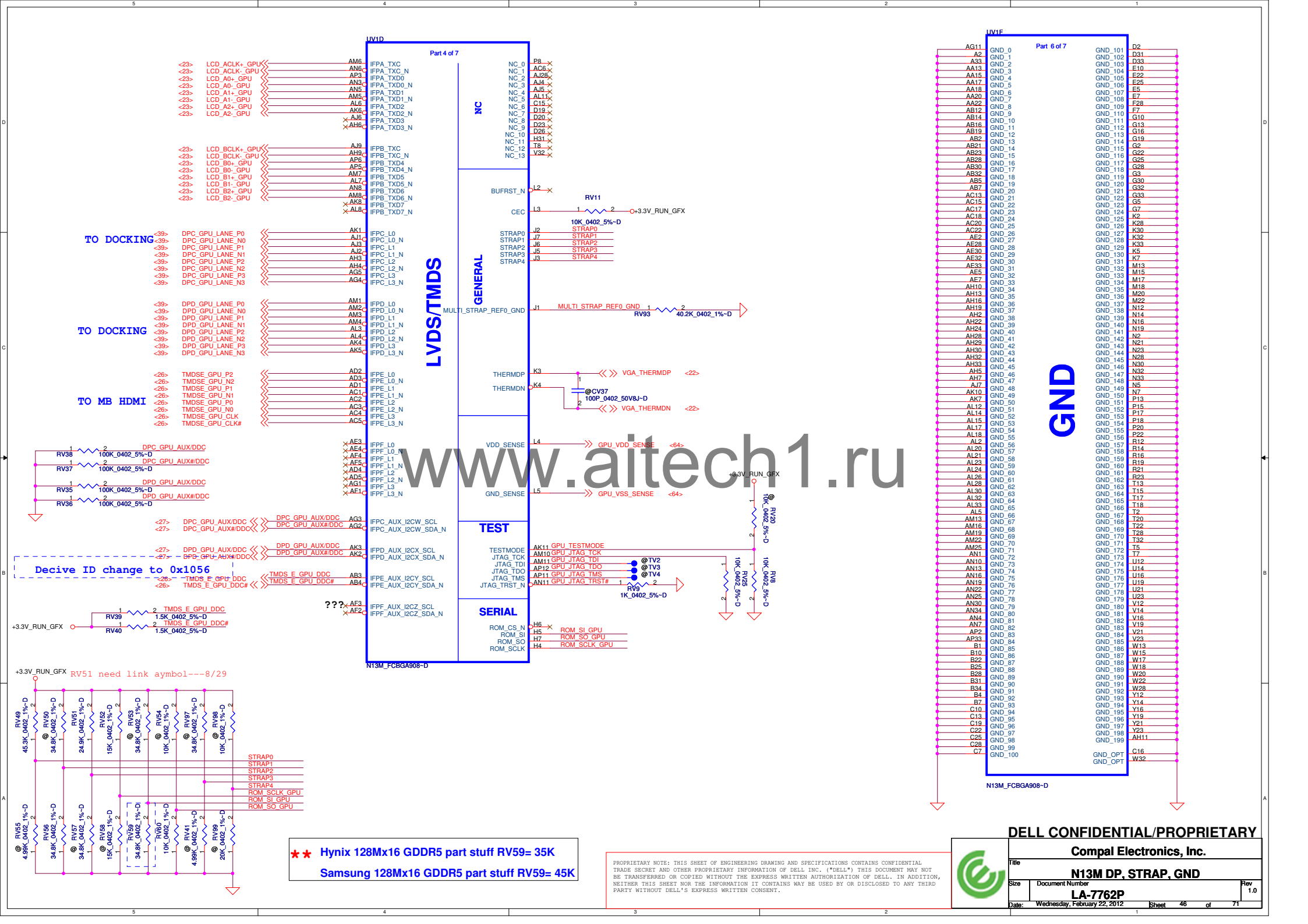
UV1D
Part 4 of 7
LVDS/TMDS
GENERAL
NC
TEST
SERIAL
N13M_FCBGA908~D
TO DOCKING
TO DOCKING
TO MB HDMI
Decive ID change to 0x1056
RV51 need link aymbol---8/29
UV1F
Part 6 of 7
GND
N13M_FCBGA908~D
www.aitech1.ru
★★ Hynix 128Mx16 GDDR5 part stuff RV59= 35K
Samsung 128Mx16 GDDR5 part stuff RV59= 45K
DELL CONFIDENTIAL/PROPRIETARY
Compal Electronics, Inc.
N13M DP, STRAP, GND
LA-7762P
Wednesday, February 22, 2012
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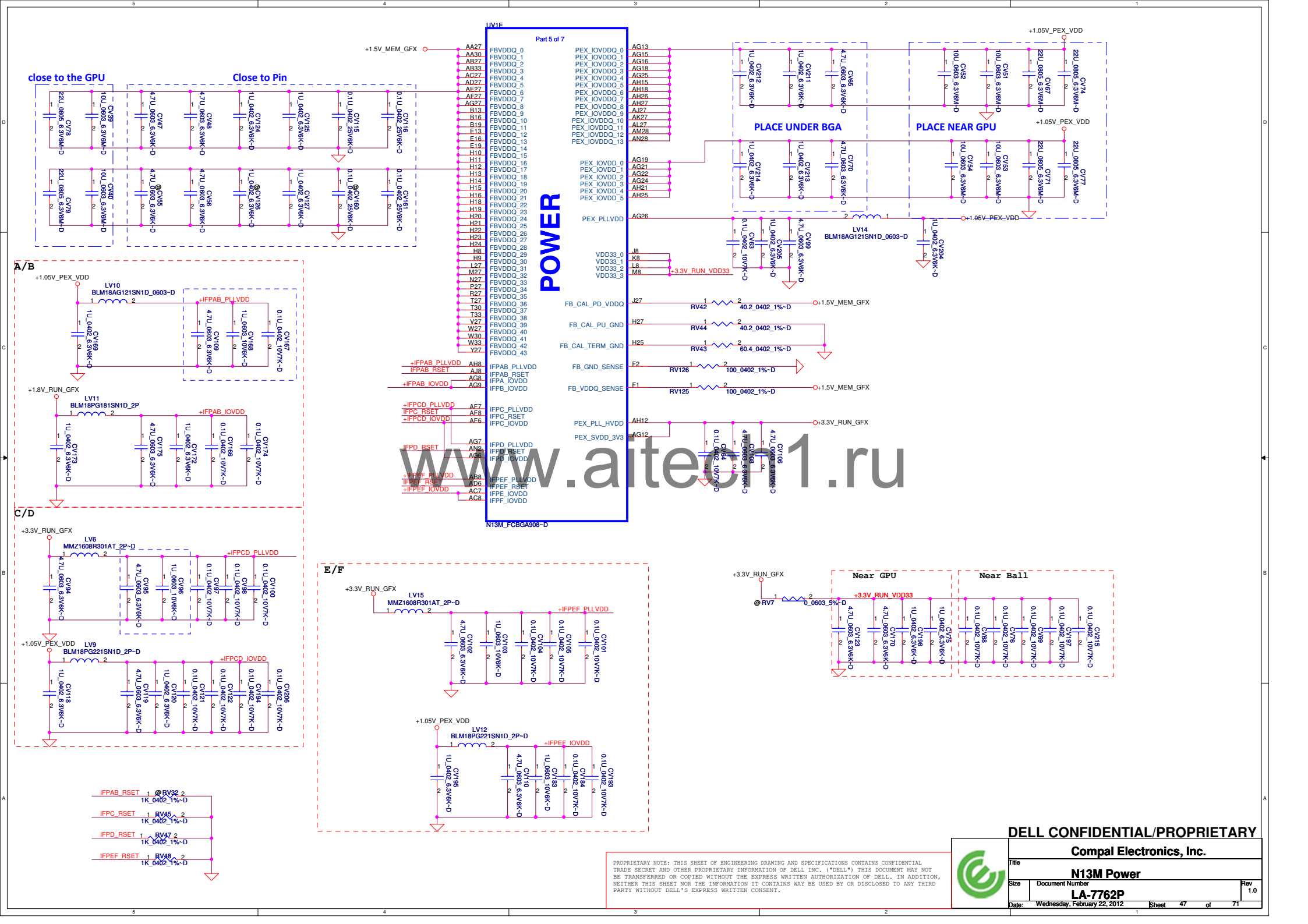

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Compal Electronics, Inc.

Title: N13M Power

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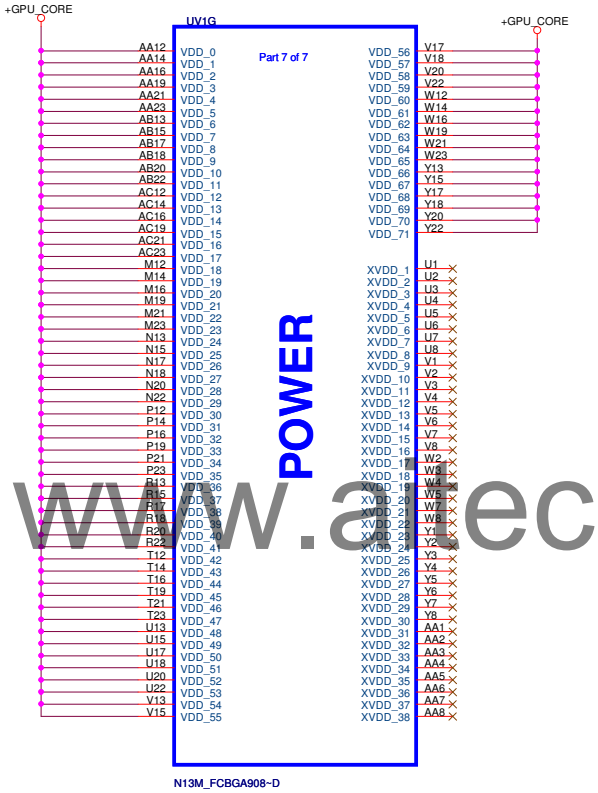
Caps on Power Side



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Compal Electronics, Inc.	
Title	N13M Power GFX Core
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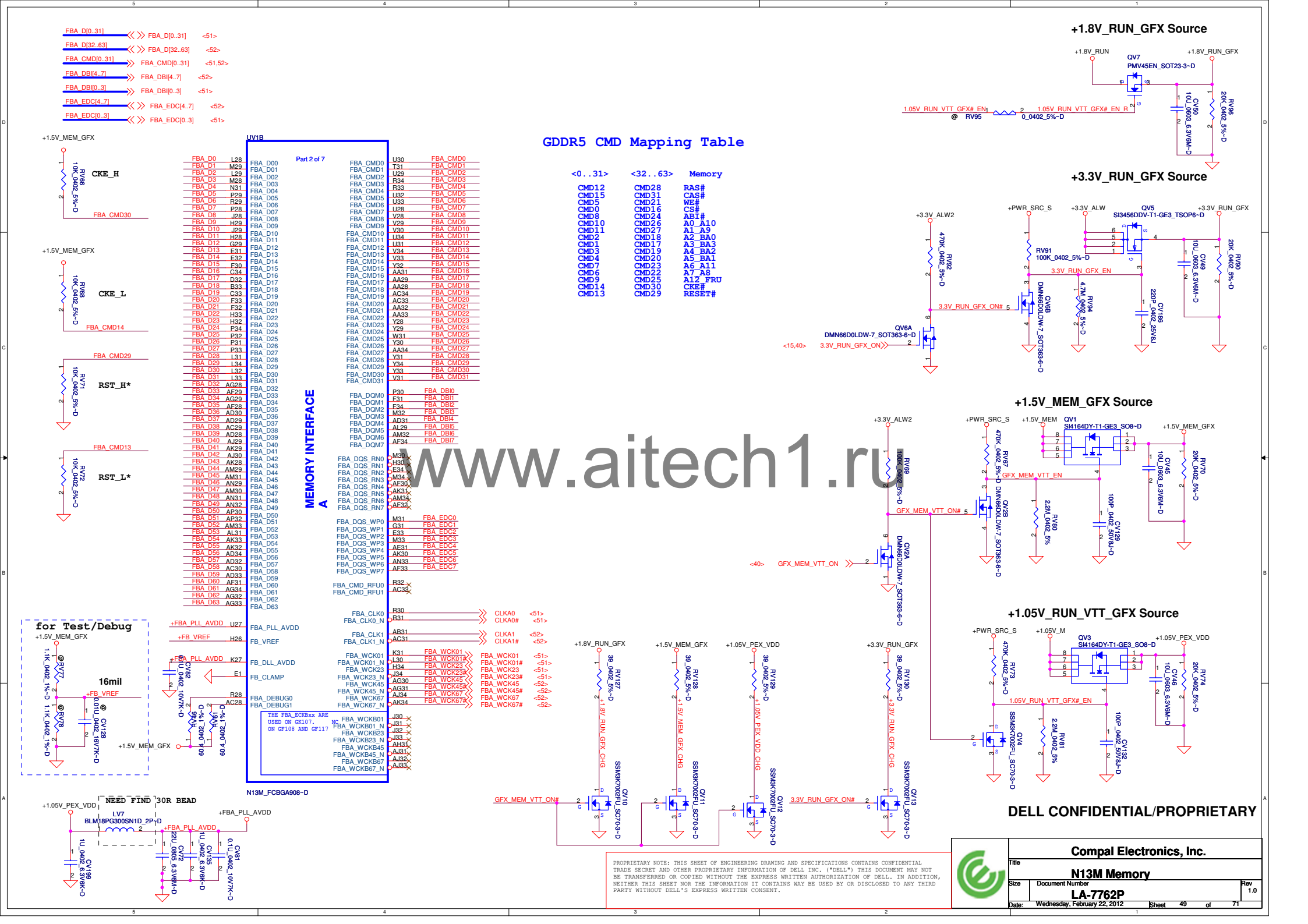
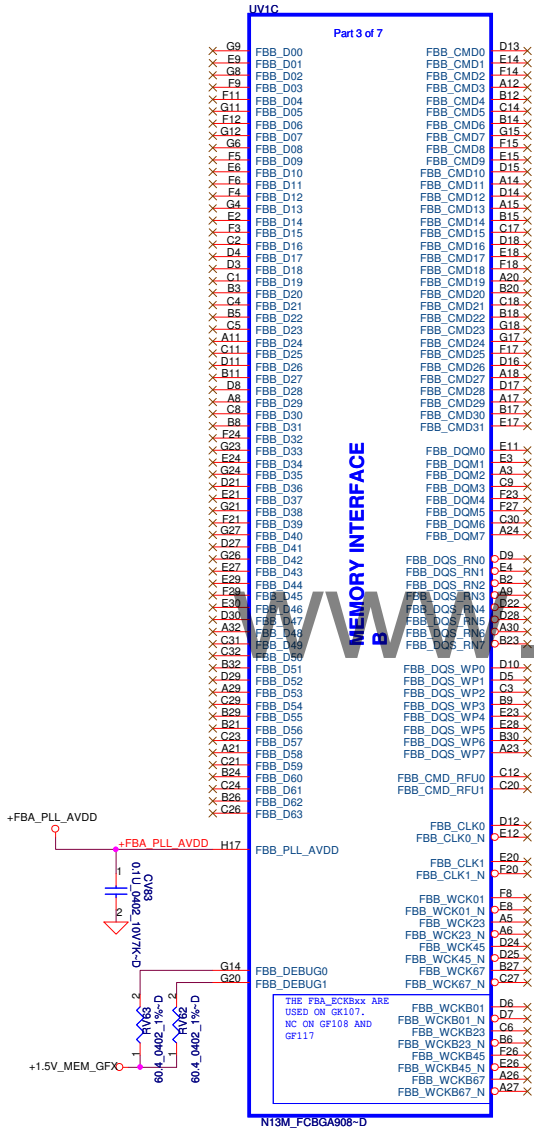


CHANNEL-B NOT TO USE, NEED TO BE DISABLED



Compal Electronics, Inc.

Title: N13M Memory (2)

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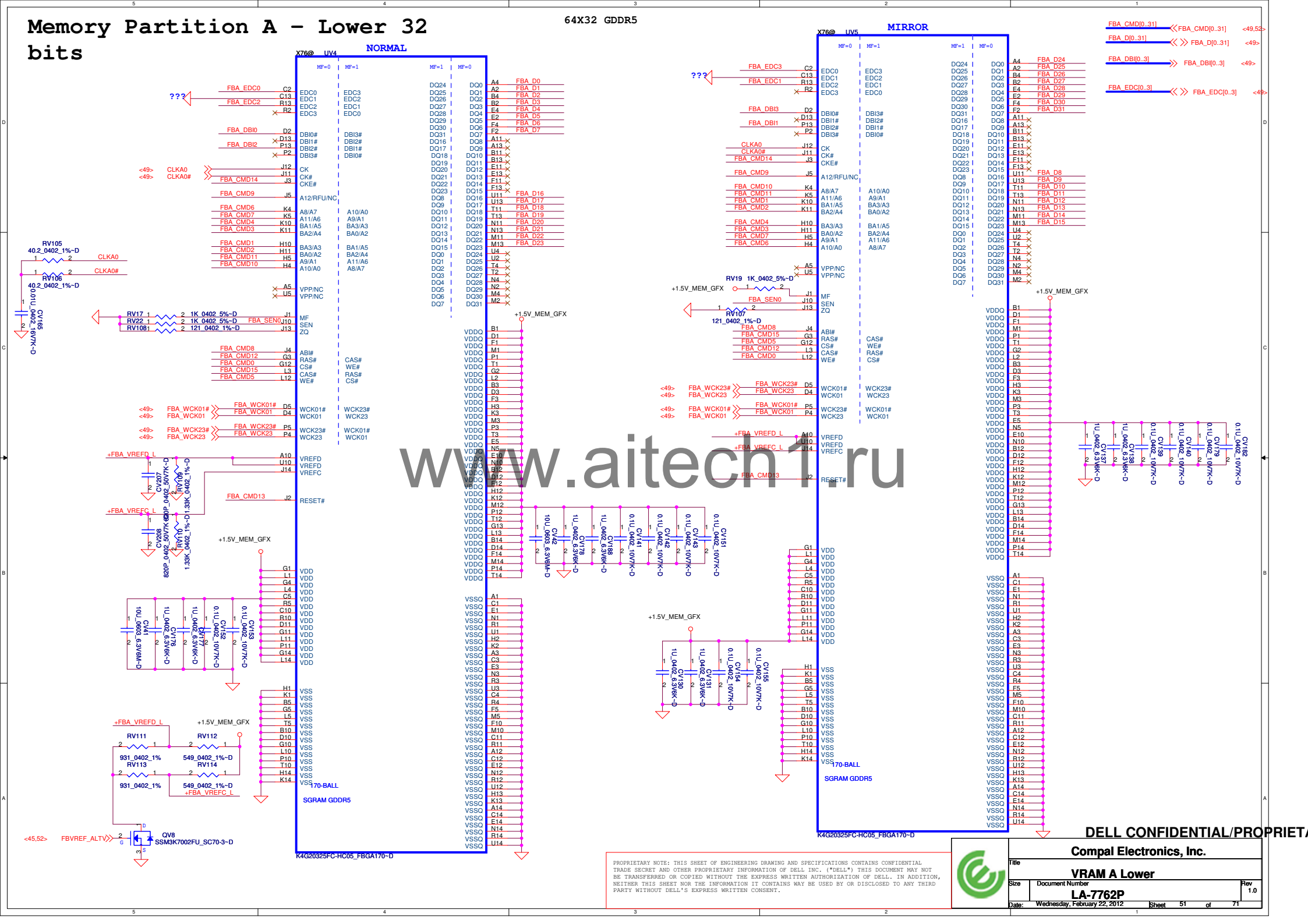
Memory Partition A - Lower 32 bits

64X32 GDDR5



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Compal Electronics, Inc.

Title: VRAM A Lower

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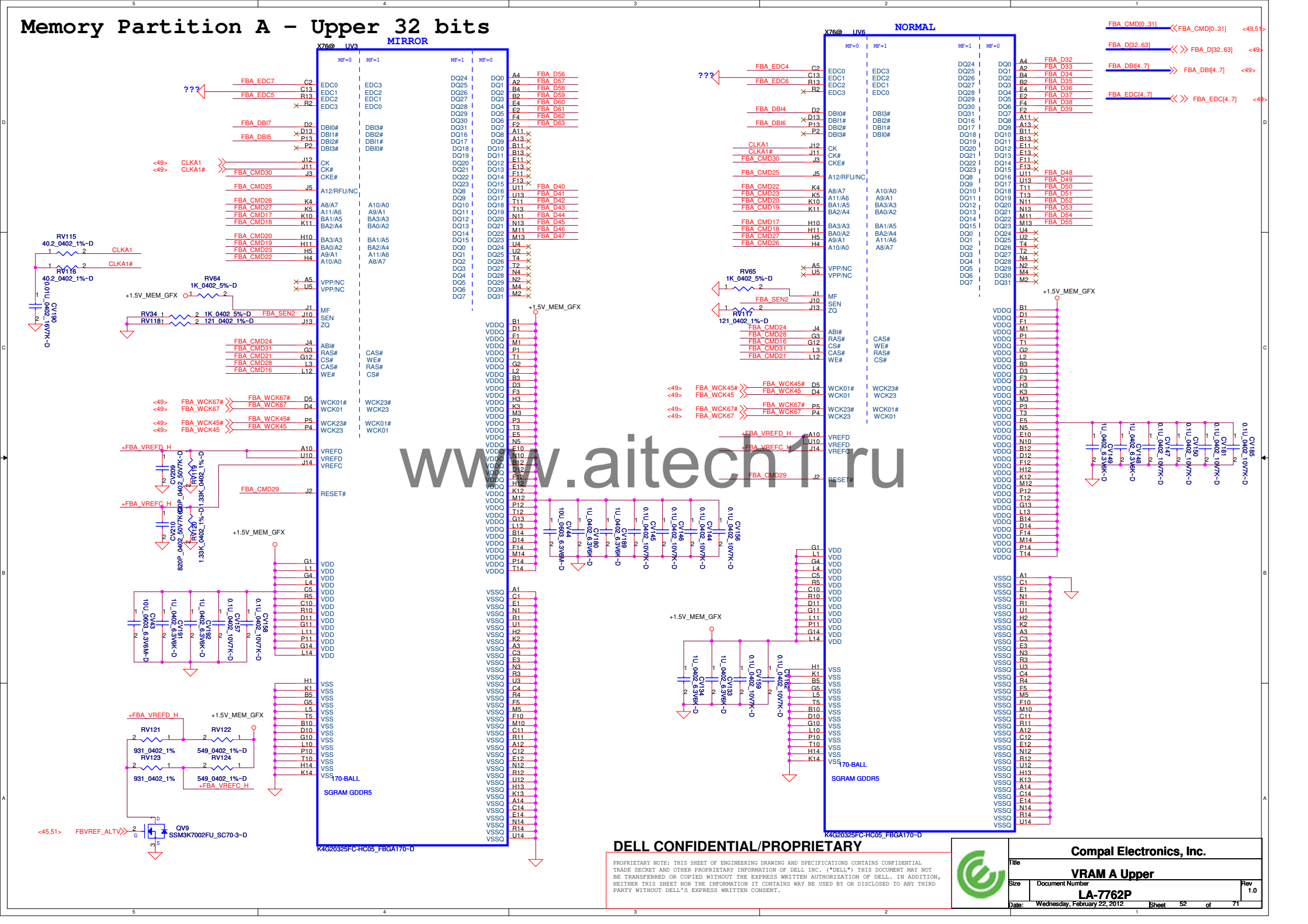
Memory Partition A – Upper 32 bits



Compal Electronics, Inc.

Title: VRAM A Upper

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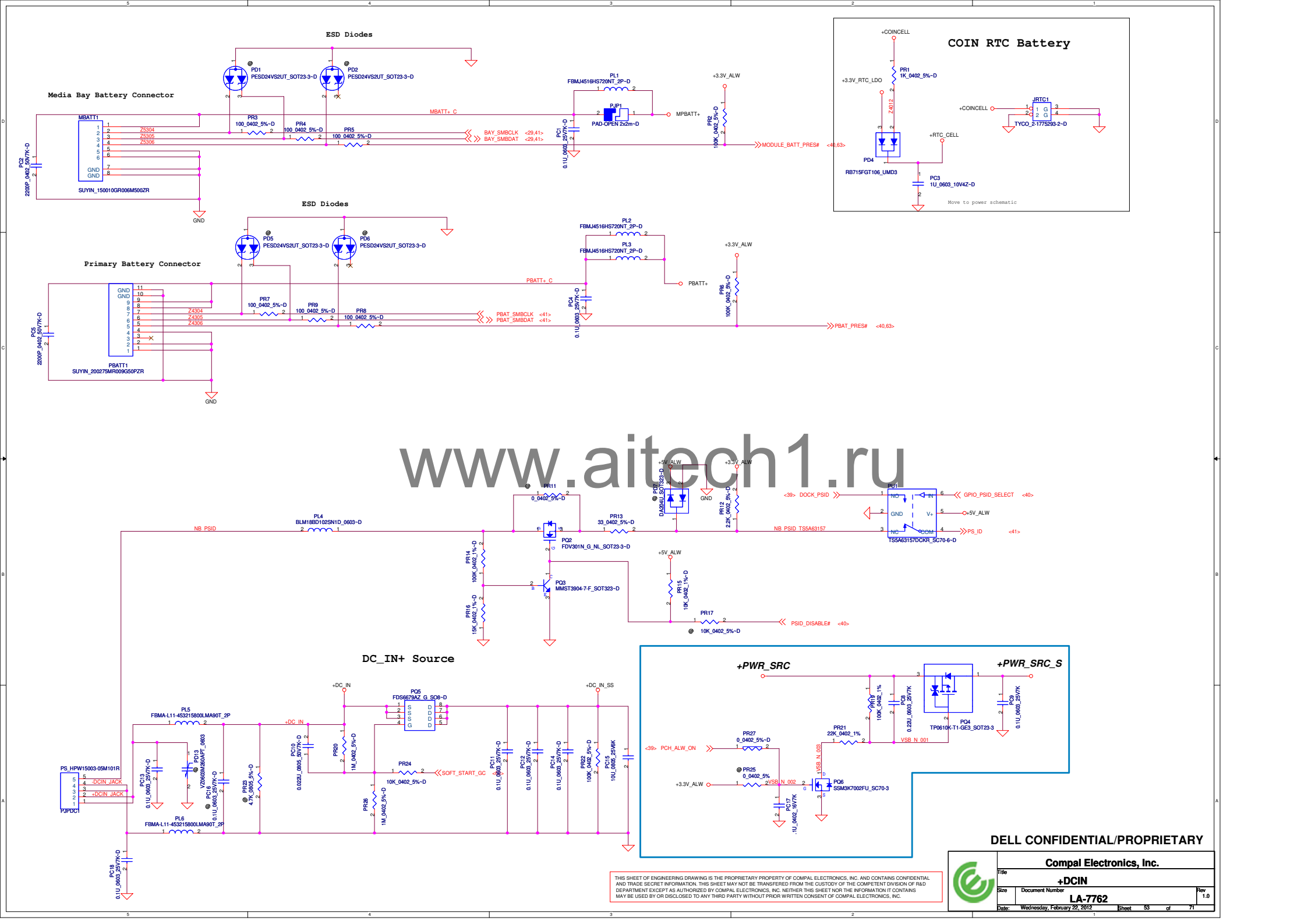

Compal Electronics, Inc.			
Title: +DCIN			
Size	Document Number: LA-7762		Rev: 1.0
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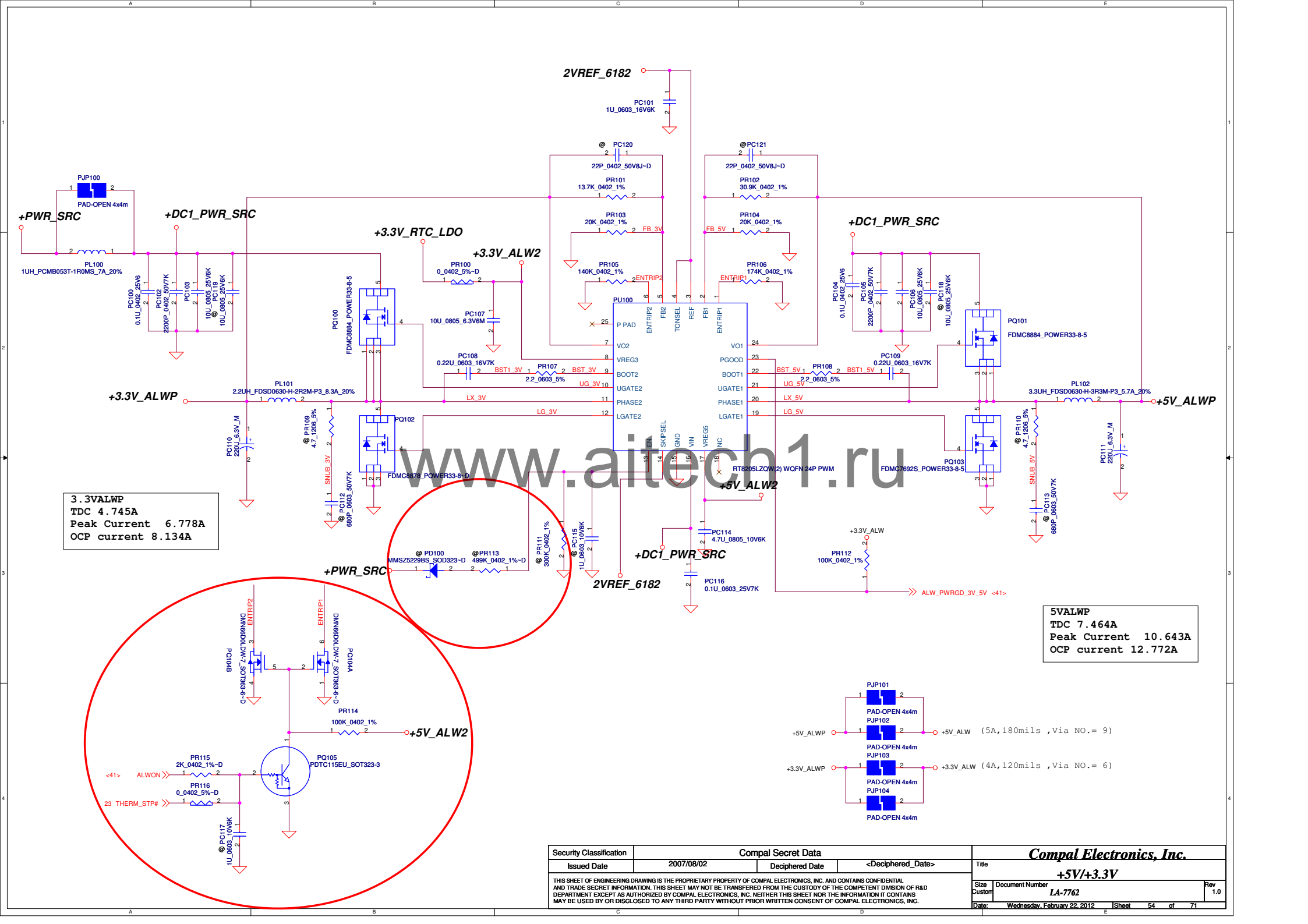

Security Classification	Compal Secret Data		
Issued Date	2007/08/02	Deciphered Date	<Deciphered_Date>

Compal Electronics, Inc.			
Title	+5V/+3.3V		
Size: Custom	Document Number: LA-7762		Rev: 1.0
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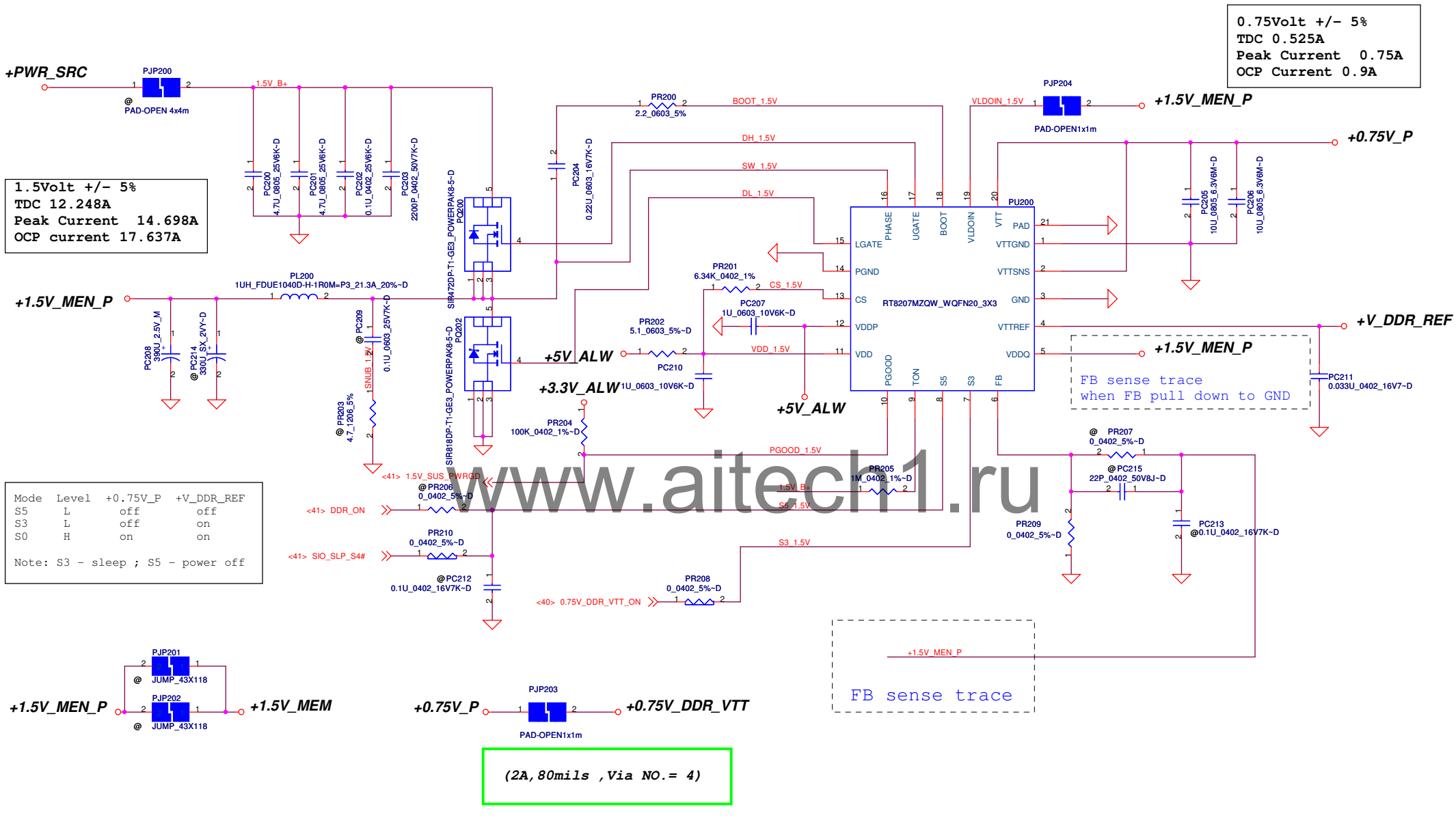

Compal Electronics, Inc.		
Title	+1.5V_MEN/+0.75V_DDR_VTT	
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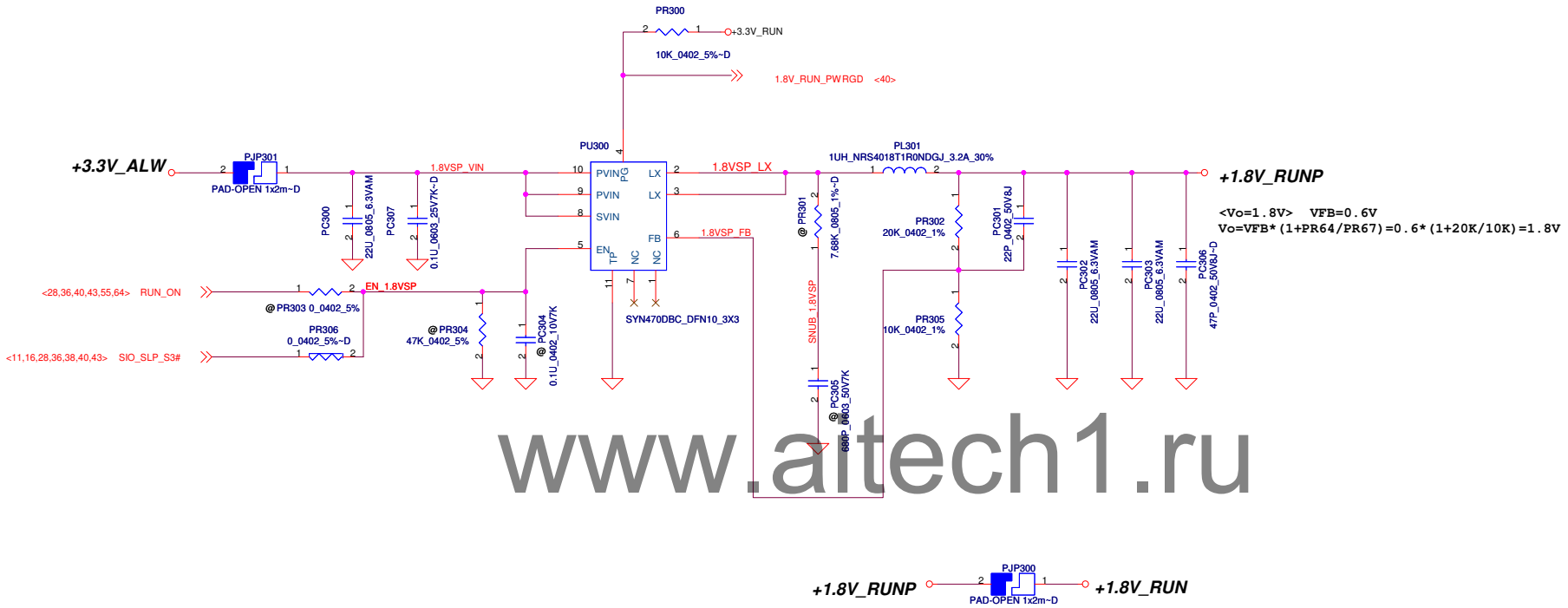
1.8Volt +/-5%
TDC 0.81A
Peak Current 1.157A
OCP current 1.388A

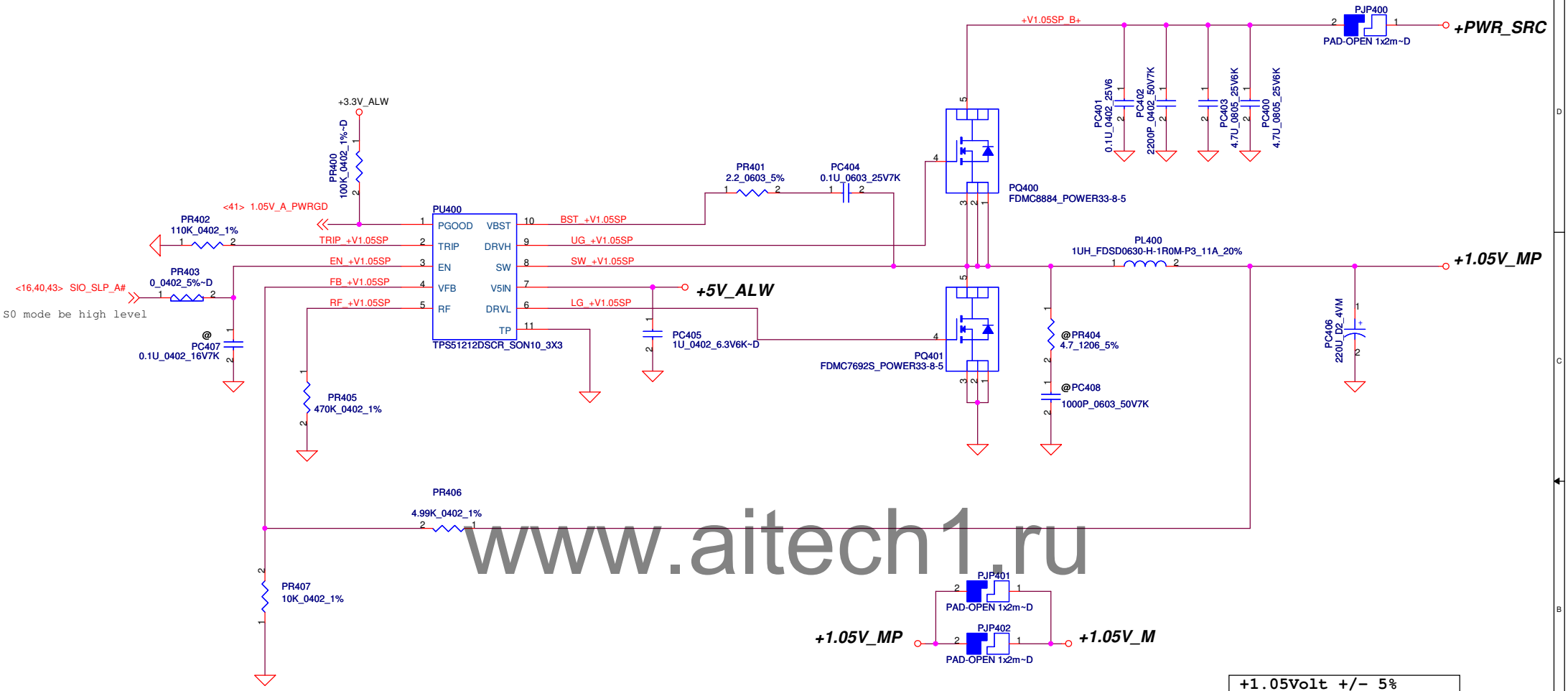


Compal Electronics, Inc.

Title: +1.8V_RUN

Size | Document Number: LA-7762 | Rev: 1.0

Date: Wednesday, February 22, 2012 | Sheet 56 of 71



+1.05Volt +/- 5%
TDC 6.78A
Peak Current 9.59A
OCP current 11.51A

Compal Electronics, Inc.

Title: +1.05V_M

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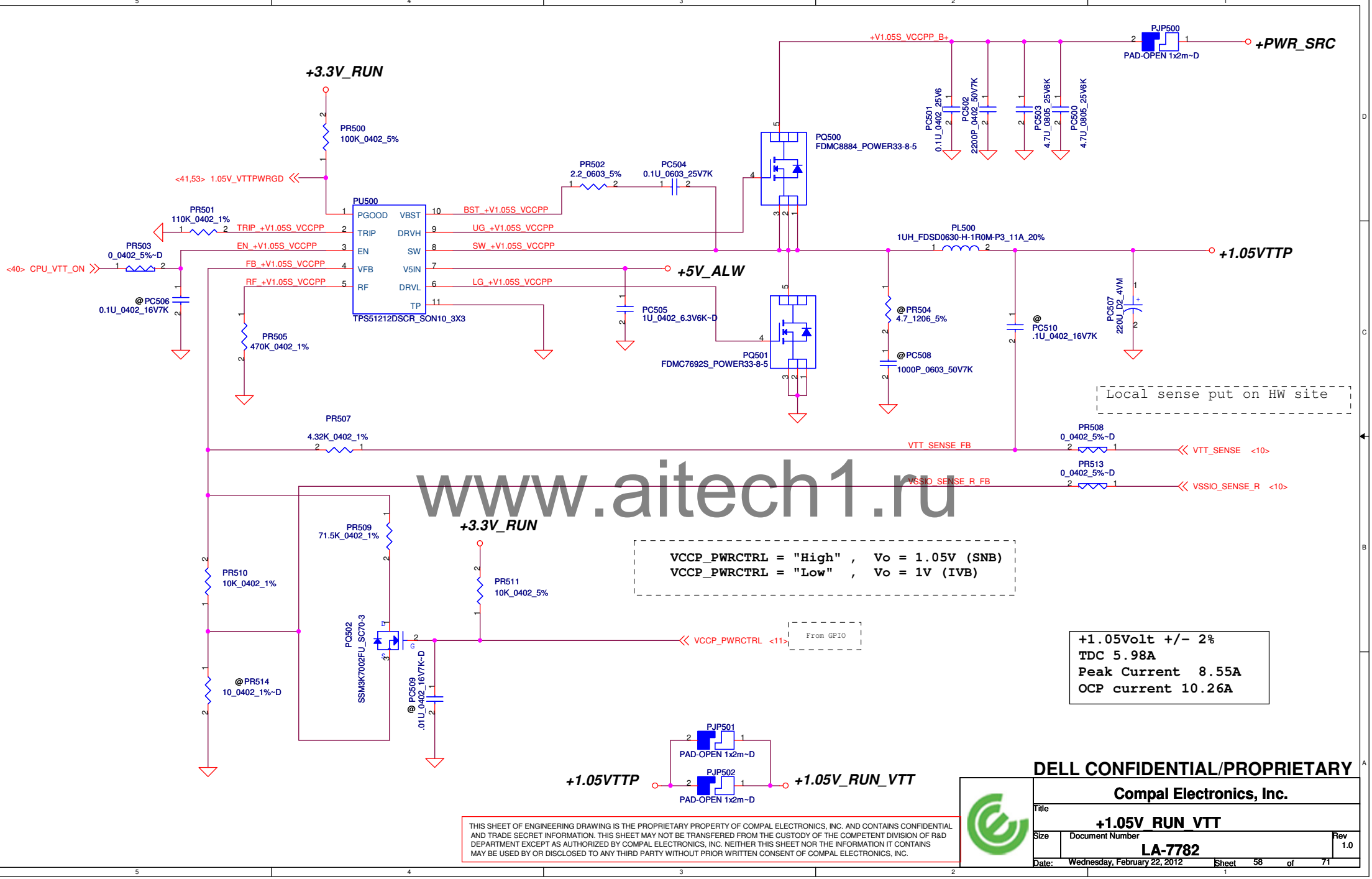

Compal Electronics, Inc.

Title: +1.05V_RUN_VTT

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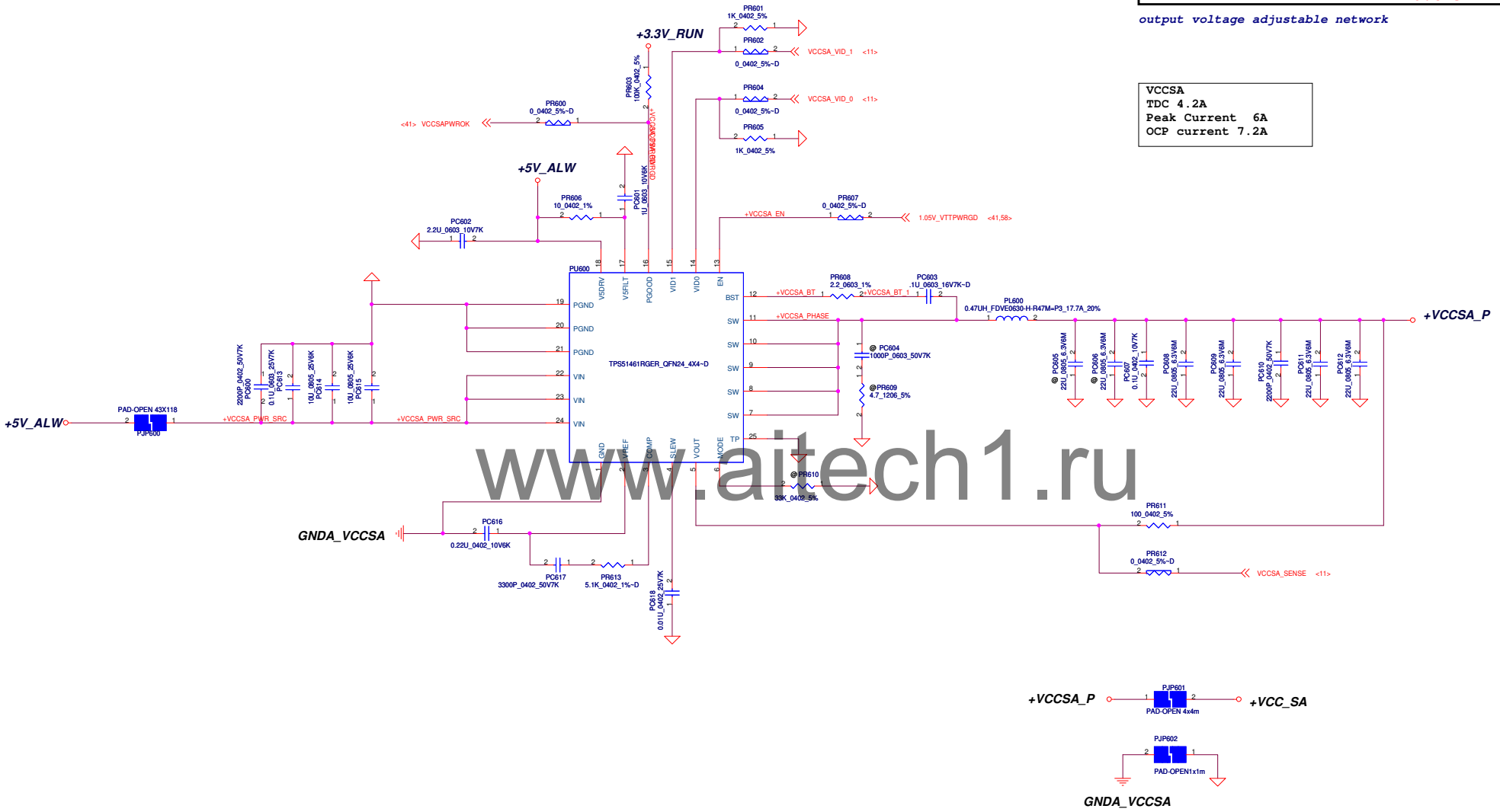
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

VCCSA
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



Compal Electronics, Inc.
Title: +VCC_SA
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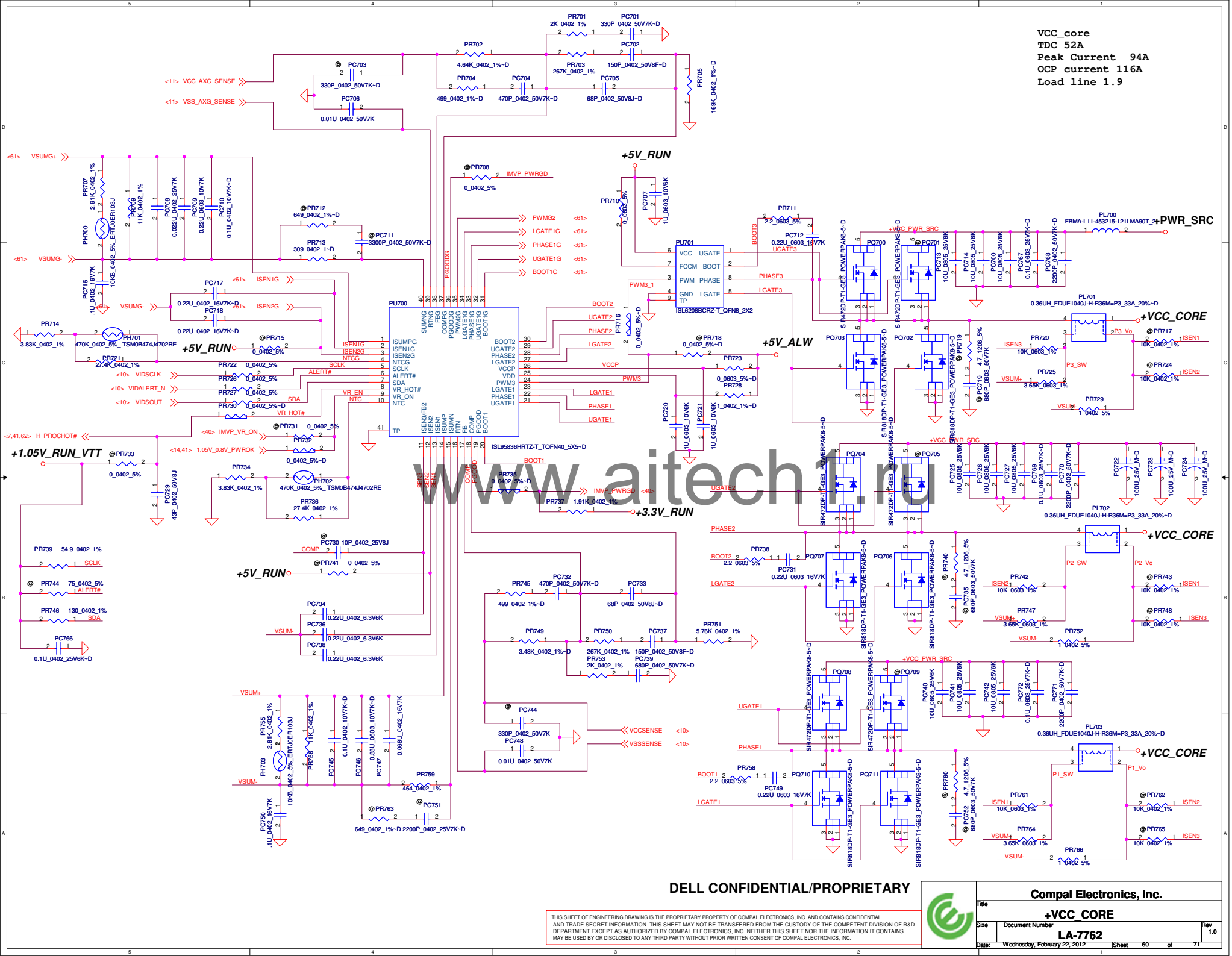
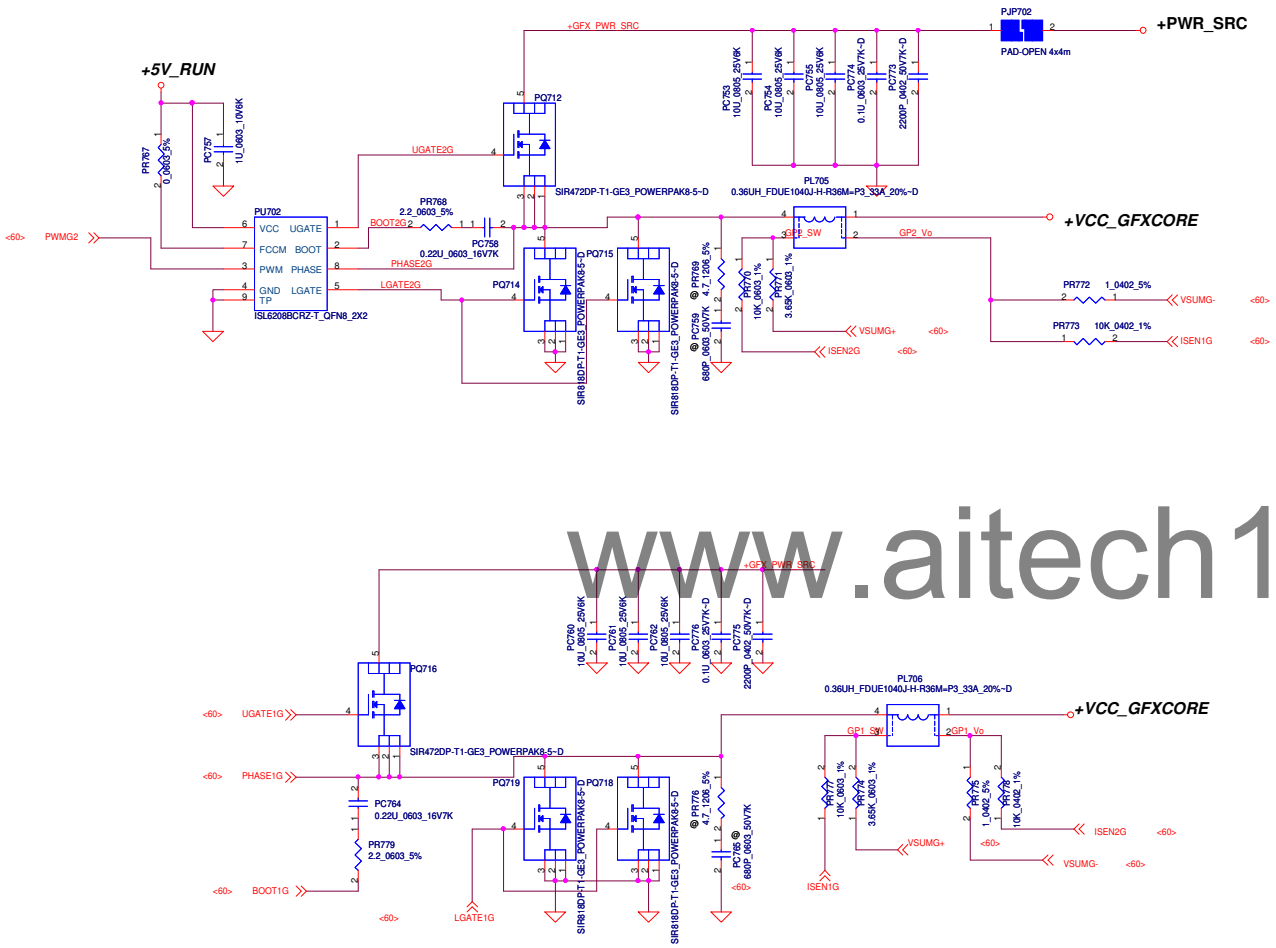


VCC_GFXCORE
TDC 38A
Peak Current 46A
OCP current 57.18A
Load line 3.9



Title: +VCC_GFXCORE

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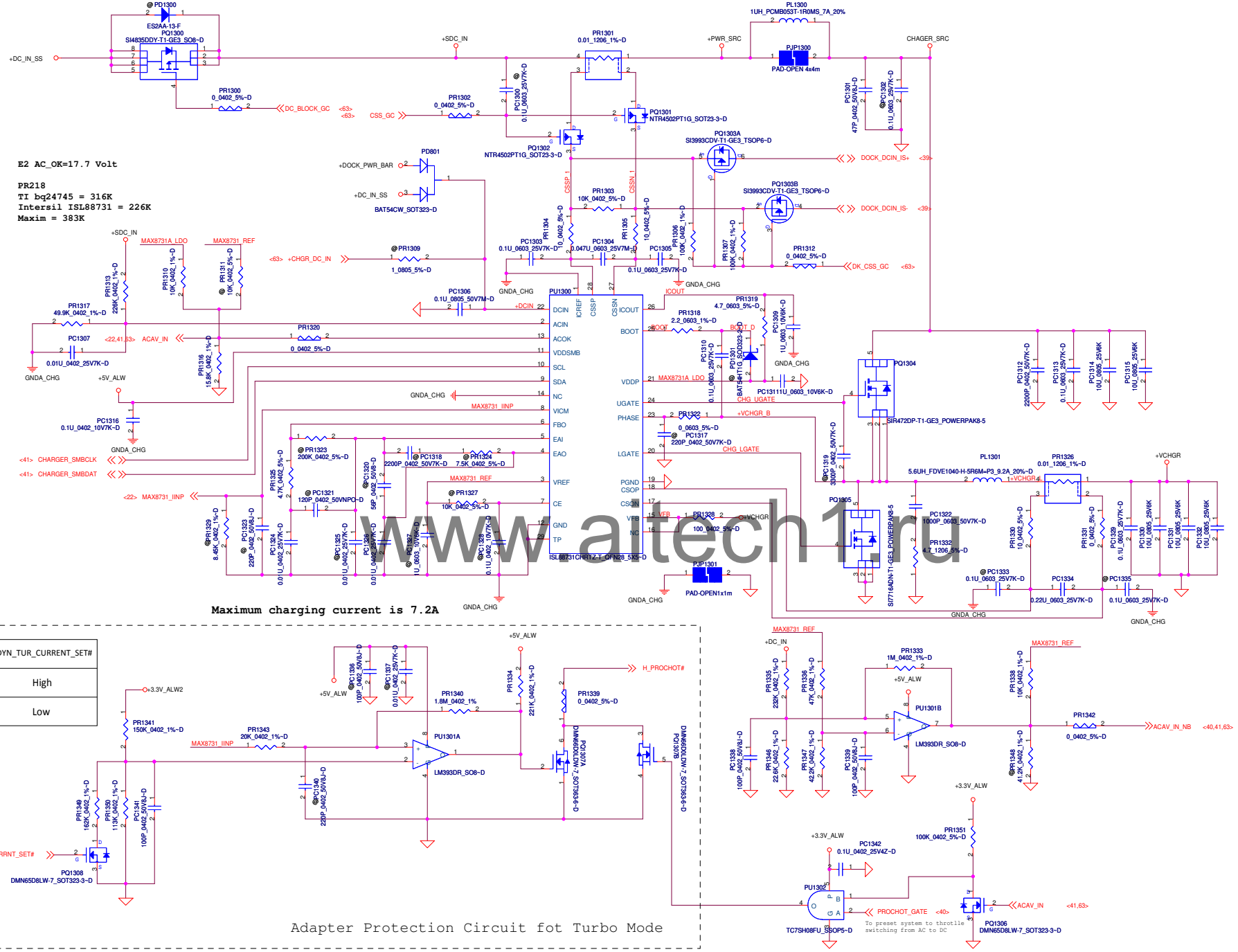

	DYN_TUR_CURRENT_SET#
90W	High
130W	Low

Compal Electronics, Inc.		
Title: Charger		
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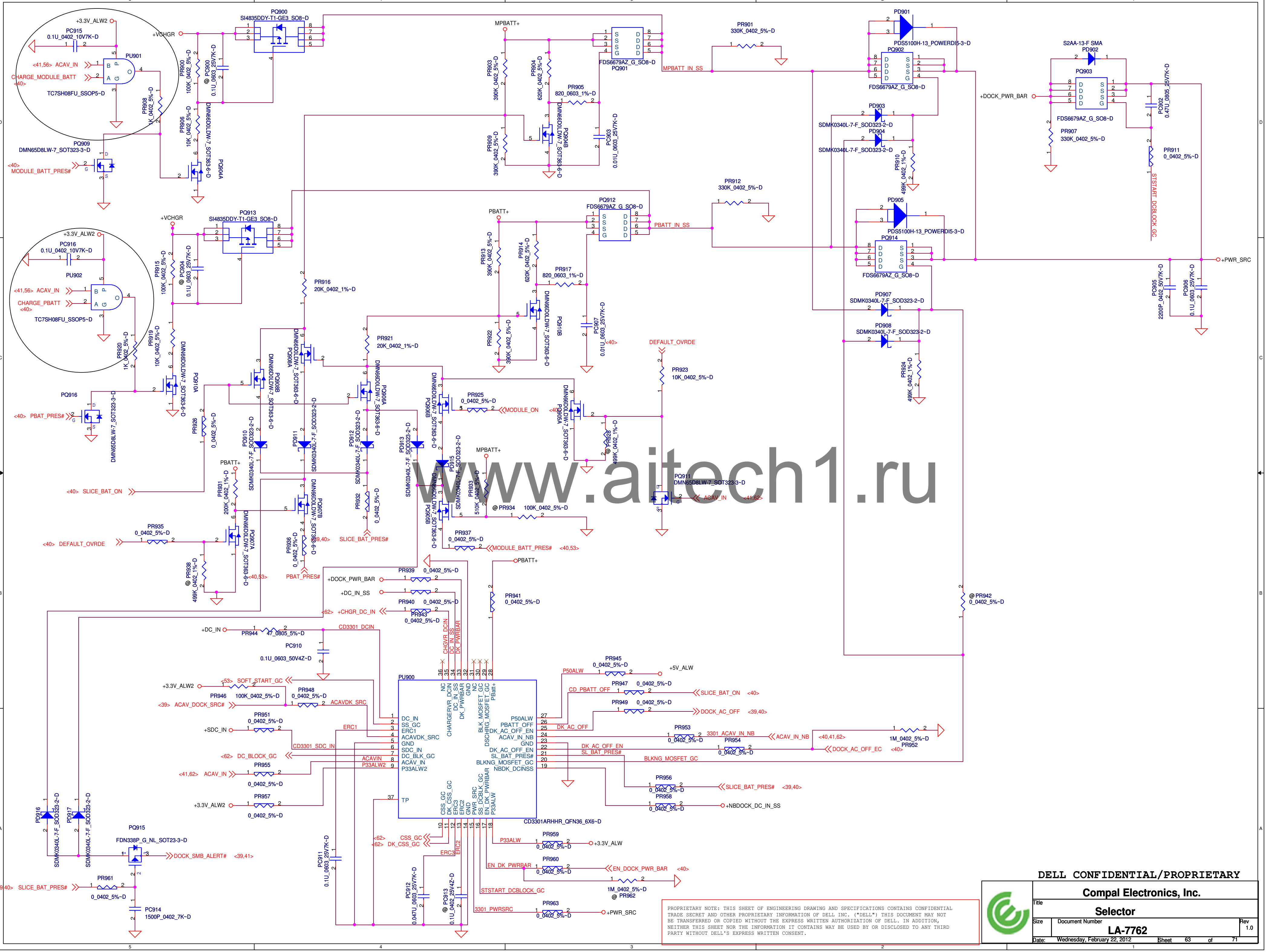

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Compal Electronics, Inc.	
Title	Selector
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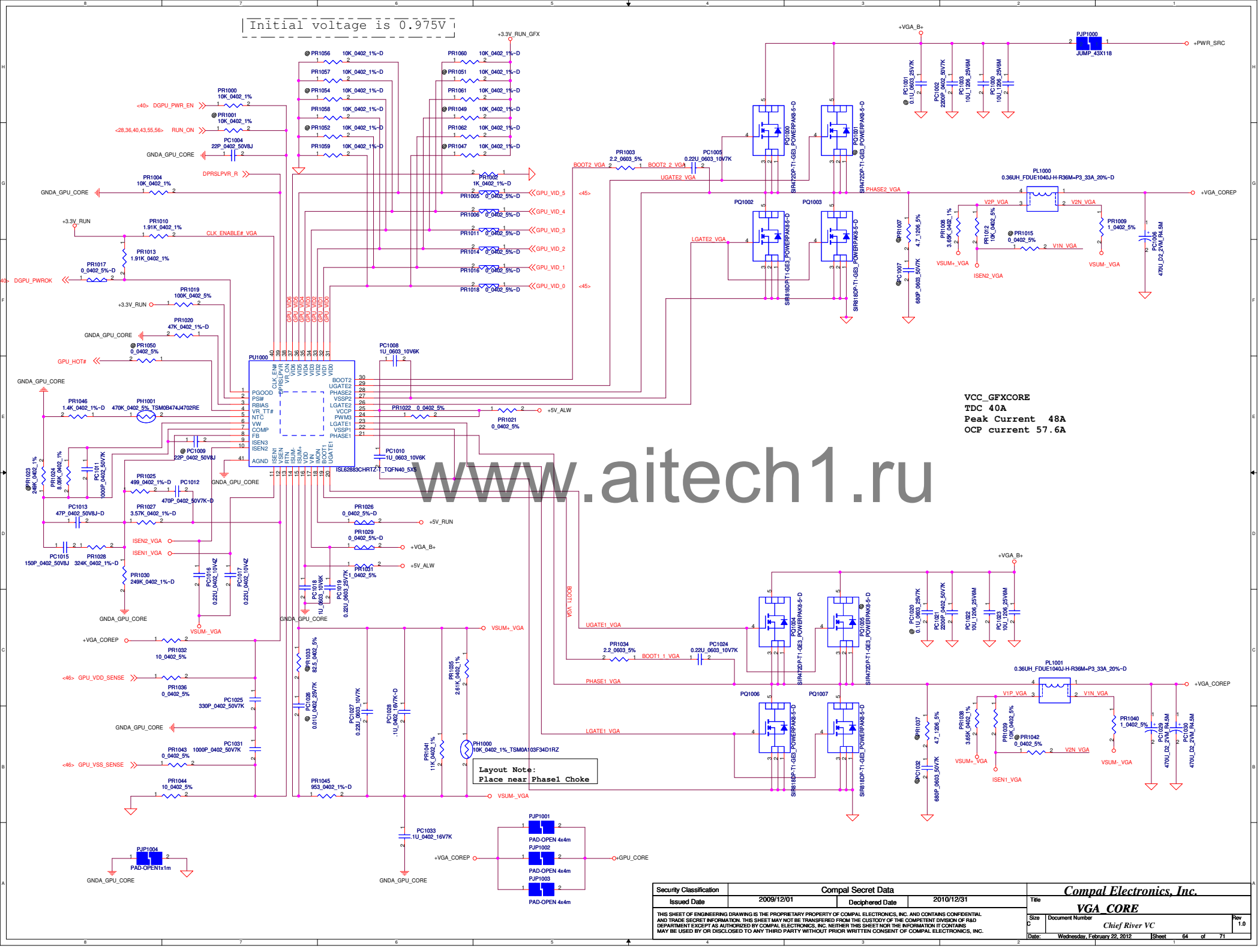

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

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Compal Electronics, Inc.

Title: VGA_CORE

Size	Document Number	Rev
C	Chief River VC	1.0

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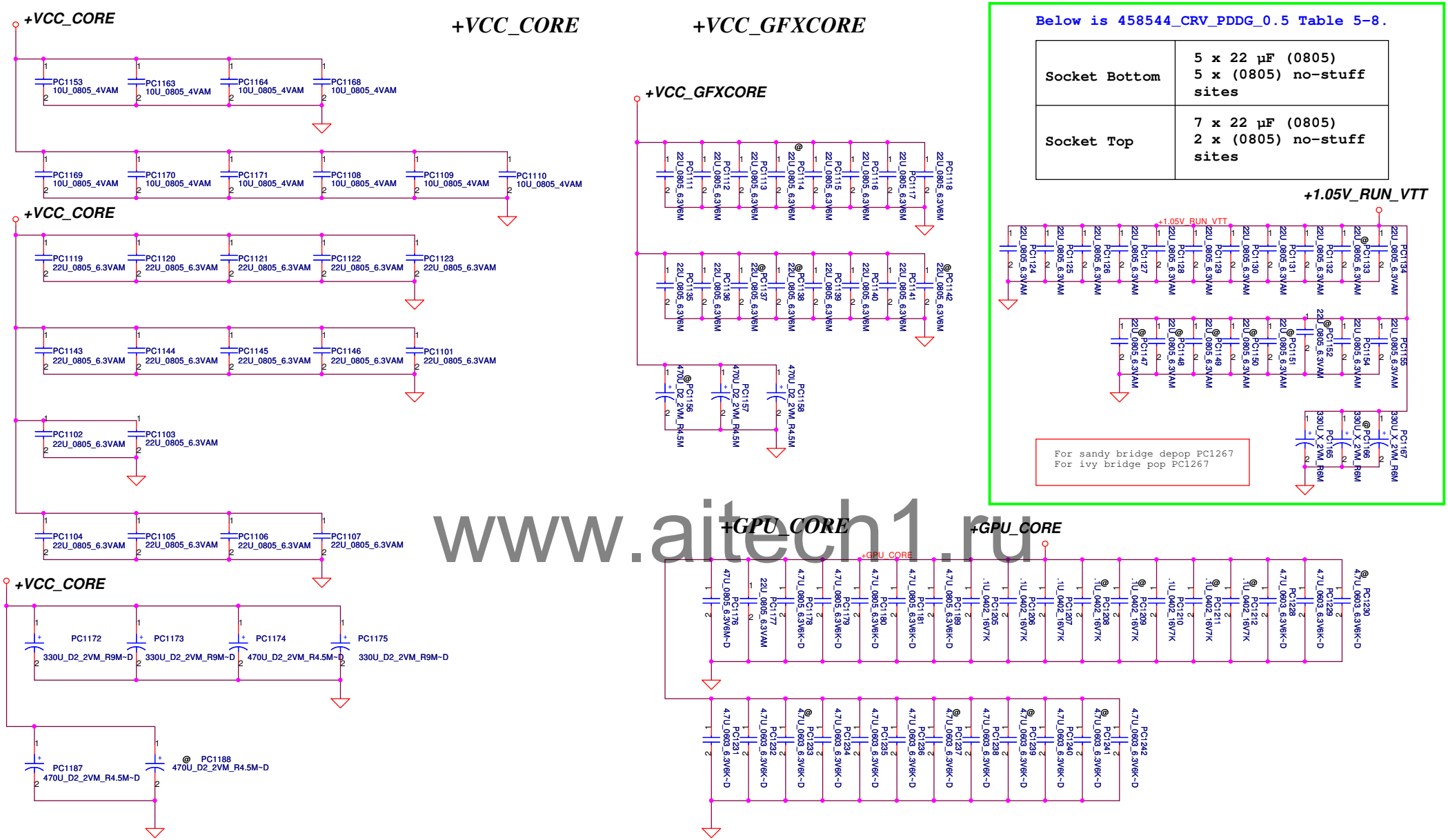

Compal Electronics, Inc.

Title: PROCESSOR DECOUPLING

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	46	HW	6/21/2011	NV	NV strap setting update.	1. Stuff RV51,RV60,RV52,RV59. 2. Not Stuff RV53,RV54,RV57,RV97,RV99. 3. Change RV52 to 15K Ω. 4. RV53 with 45.3K 1% for Samsung 64Mx32; with 34.8K 1% for Hynix 64Mx32.	X01
2	37	HW	6/21/2011	COMPAL	USB3.0 & E-SATA behavior error.	U48 pin 10 & pin6 swap, and pin4 & pin5 swap.	X01
3	41	HW	6/21/2011	COMPAL	Modify Touch Pad circuit	De-pop R1162.	X01
4	11	HW	6/21/2011	INTEL	Follow INTEL check list Rev1.5.	RC99 ,RC100 change to 100 Ω	X01
5	31	HW	6/21/2011	IDT	IDT request.	PJP62 change to "JUMP_43X118".	X01
6	29	HW	6/21/2011	COMPAL	Modify WWAN circuit.	JMINI1 pin1 contact to PCIE_WAKE#.	X01
7	34	HW	6/21/2011	COMPAL	Follow E4 VC +3.3V_SUS Source circuit .	Reserve SIO_SLP_S4# contact to Q53 pin2.	X01
8	42	HW	6/27/2011	COMPAL	Leverage 14" schematic to modify Codec circuit.	Remove R167 & R178 (0 Ω) .	X01
9	30	HW	7/18/2011	COMPAL	Leverage 14" schematic to modify PCH_GPIO16 pull-up resistor.	Change RH272 from 8.2KΩ to 10KΩ.	X01
10	18	HW	7/18/2011	COMPAL	Leverage 14" schematic to modify CAM_MIC_CBL_DET# pull-up resistor.	Change RH331 from 8.2KΩ to 10KΩ.	X01
11	43	HW	7/18/2011	COMPAL	Load SW sources output rising time mismatch and COS,cost concern.	Change back to E3 +3.3V/5V_RUN discrete solution	X01
12	15,45	HW	7/28/2011	COMPAL	bass on vender measure crystal EA by pass.	CH18,CH19 change to 6.8pF. CV34,CV35 change to 15pF.	X01
13	35	HW	7/28/2011	COMPAL	Follow INTEL check list(Rev1.5) change PCH GPIO52(PCIE_MCARD2_DET#) pull up resistor to 10KΩ.	Change R695 from 100K to 10Kohms.	X01
14	45	HW	7/28/2011	COMPAL	DGPU_PEF_RST abnormal during power on.	Change UV14 power to +3.3V_ALW.	X01
16	33	HW	7/28/2011	COMPAL	INTEL power sequence fail on T13(+1.8V_RUN to H_CPUPWRGD assert) due to USH move to sub-board but "USH_PWR_STATE#" no PU/PD for default.	Add R1640, 1M ohms pull down for USH_PWR_STATE# at M/B side	X01
17	11	HW	7/28/2011	COMPAL	Follow INTEL check list Rev1.5 for "VCCIO_SEL" , series resistor no stuff .	De-pop RC140	X01
18	41	HW	7/28/2011	COMPAL	Change board ID to X01	Change R875 to 130Kohms	X01
19	24	HW	7/28/2011	COMPAL	VCC tolerance of U3 is changed to 3.3V	Change U3 to SA00002VK00	X01
20	24	HW	7/28/2011	COMPAL	DELL requests PWM control flexibility.	Reserve D71 for PWM,but de-pop.	X01
21	20,43	HW	7/28/2011	COMPAL	Turn on +5V_ALW_PCH MOSFET Vgs less than cut-in voltage in battery mode.	Add control circuit for +5V_ALW_PCH	X01

Compal Electronics, Inc.
Title: EE P.I.R (1/4)
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
22	40	HW	7/28/2011	SMSC	SMSC no support function for LPC_LDRQ0#.	Delete net, LPC_LDRQ0#. Leave LDRQ0# no connection on both of 5048 and PCH side	X01
23	30	HW	7/28/2011	IDT	CODEC is change to 92HD93.	Pop R162~R166 and de-pop U73.	X01
24	30	HW	7/28/2011	IDT	Co-lay 92HD93 circuit for I2S BUS control.	Reserve 0 Ω(R1641) to connect Codec Pin48 of the Codec and EN_I2S_NB_CODEC#.	X01
25	43	HW	8/3/2011	COMPAL	Modify +1.5V_RUN load switch circuit for POWER team suggestion.	Change Q59 from NTGS4141NT1G to AO4728L.	X01
26	16	HW	8/3/2011	COMPAL	Follow INTEL Power down sequence Tc timing fail(BITS:DF493966).	Add AND Gate(TC7SH08FU) input connect PM_APWROK & SIO_SLP_A# , and output connector PM_APWROK_R.	X01
27	42	HW	8/4/2011	COMPAL	Reset IC threshold voltage issue	Change U4 to RT9801A (threshold adjustable).	X01
28	17	HW	8/4/2011	COMPAL	Intel Review Feedback for PCH_GPIO3.	POP RH332.	X01
29	30	HW	8/4/2011	COMPAL	Co-lay 92HD93 with ALC290	Modify codec schematics	X01
30	14	HW	8/4/2011	COMPAL	SPI debug connector interfere power CAP(PC208) change connector type.	Change JSPI1 connector to SP01001DQ00.	X01
31	11	HW	8/5/2011	COMPAL	CH94 and CH95 to D2 size for cost concern	Change CH94 and CH95 from SGA0000170L to SGA00004L0L	X01
32	44	HW	8/11/2011	COMPAL	White light LED brightness is abnormal	change the resistor value: R934 change to 1K,R938 & R955 change to 1.8K,R939 change to 1.4K,R949 & R958 change to 620 and R957 change to 220.	X01
33	11	HW	8/12/2011	COMPAL	S3 resume issue.	Pop RC79 and de-pop RC82.	X01
34	37	HW	8/29/2011	COMPAL	USB3.0 Tx AC coupling follow CRBboard.	change C412 & C413 to 0.1uF.	X01
35	19	HW	8/29/2011	COMPAL	CRT ripple garbage display issue.	change LH1 to 1uH inductor,Change CH36 from 10uF(0603) to 22uF(0805).	X02
36	44	HW	8/29/2011	COMPAL	White light LED brightness is abnormal.	change the resistor value: R934 change to 1K,R938 & R955 change to 1.8K,R939 change to 1.4K,R949 & R958 change to 620 and R957 change to 220.	X02
37	30	HW	9/28/2011	IDT	Audio no sound issue in Dalmore 15 UMA.(BITS:DF504001).	Add C-R snubber circuit,C973~C976(2200P),R1658~R1661(3.3Ω).	X02
38	41	HW	9/28/2011	COMPAL	EC has internal pull up for volume signals.	De-pop R1169, R1197, R1118.	X02
39	43	HW	9/28/2011	COMPAL	+3.3V_RUN boot leakage issue.	Pop Q69 & R929.	X02
40	43	HW	9/29/2011	COMPAL	DMN3030LSS-13 poor soldering issue.	change Q55,Q61 to AO4478L.	X02
41	40	HW	9/29/2011	COMPAL	SMSC change ECE5048 Pin A23 to GPIO0.	Link ECE5048 symbol.	X02
42	41	HW	10/12/2011	SMSC	SMSC review feedback.	Reserve R1656 and R1657 100Kohms to GND for I2S disabled.	X02
43	43	HW	10/12/2011	COMPAL	+3.3/5V_RUN inrush curren issue with 470pF.	Change C763 and C766 form 470pF to 220pF.	X02

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
44	30	HW	10/12/2011	COMPAL	Remove ALC290 co-lay circuit.	Remove R1646, C1164, R1644, R1643, R1642, R171, C1204, C1205, R1647, C1165, R1648 and R1645.	X02
45	40	HW	10/13/2011	COMPAL	When suspend/resume cycles, wireless SW GPIO IRQs keeps giving	Add R771 pulling up to +3.3V_ALW for WIRELESS_ON#/OFF and de-pop R766.	X02
46	42	HW	10/13/2011	COMPAL	Chane reset IC to RT9818A-44GU3.	Update U4 symbol and add R1629 for backup of inrush prevention. Change RSMRST# pull up with 100Koms. Pop R1655 and de-pop R1623.	X02
47	42	HW	10/13/2011	COMPAL	Change board ID to X02.	Change R875 to 62Kohms.	X02
48	34	HW	10/13/2011	COMPAL	EMI request to change SD CLK series R.	R676 is changed from 33ohms to 10ohms.	X02
49	ALL	HW	10/13/2011	COMPAL	For cost saving.	Change 0 ohm resistor to short pad.	X02
50	44	HW	10/13/2011	COMPAL	DFX request to change CILP PAD.	Change CLP1 PAD from "79X138" to "110X138" .	X02
51	22	HW	10/21/2011	COMPAL	VSET Setting change Tp from 88 degree to 93 degree.	change R406 from 953Ω to 1.33KΩ.	X02
52	17,35.	HW	11/08/2011	COMPAL	PCH GPIO52 changed to be free.	De-pop R725, remove R695 and add RH359.	X02
53	ALL	HW	11/08/2011	COMPAL	For cost saving.	Change 1Kohms +-1% to +-5% except RC78, RC80, RC81, RC84, RV32, RV45, RV47 and RV48.	X02
54	11,43	HW	11/14/2011	COMPAL	AO4728L leakage issue.	Change QC3 and Q59 to AO4304L (SB00000RV00).	X02
55	33	HW	11/14/2011	COMPAL	+3.3V_RUN Giltch when AC plugin.	Add D87, R1666 and R1665 for HW solution backup.	X02
56	45	HW	11/15/2011	COMPAL	pop option for GPU deeper sleep mode.	Add net name, DPRSLPVR on GPU GPIO16 and reserve RV131.	X02
57	14~21	HW	11/16/2011	COMPAL	Change PCH to C0 version.	Change UH4 to SA00005BU0L.	X02
58	39	HW	11/16/2011	COMPAL	EMI request to add 33Ω for DP port.	Add 33ohm on DPD_DOCK_LANE_P0/N0,DPD_DOCK_LANE_P1/N1,DPD_DOCK_LANE_P2/N2, DPD_DOCK_LANE_P3/N3,DPC_DOCK_LANE_P0/N0, PC_DOCK_LANE_P1/N1, DPC_DOCK_LANE_P2/N2, PC_DOCK_LANE_P3/N3.	X02
59	11,24,29, 43,49.	HW	11/16/2011	COMPAL	Change RC value at Gate of MOS Load SW to modify power rail soft start timing.	RC72 from 100K to 330K; RC143 form 330K to 1M; CC136 form 0.1u to 0.022u R412 from 100K to 470K; R1632 form 1M to 4.7M; C293 form 0.1u to 0.022u R507 from 100K to 470K; R517 form 1M to 4.7M; C400 form 0.1u to 0.022u R722 from 100K to 470K; R1625 form 1M to 4.7M; C644 form 4700p to 220p R729 from 100K to 470K; R1628 form 1M to 4.7M; C650 form 4700p to 220p R917 from 100K to 470K; R1617 form 1M to 4.7M; C770 form 4700p to 220p R920 from 100K to 470K; R1610 form 470K to 2.2M; C771 form 4700p to 470p R930 from 330K to 470K; R1611 form 470K to 1M; C773 form 2200p to 100p R906 from 100K to 470K; C763 form 2200p to 220p R912 from 100K to 470K; C766 form 470p to 220p RV73 from 100K to 470K; RV81 form 470K to 2.2M; CV132 form 2200p to 100p RV67 from 100K to 470K; RV80 form 470K to 2.2M; CV129 form 2200p to 100p RV91 from 100K to 470K; RV94 form 1M to 4.7M; CV186 form 3300p to 220p	X02
60	26	HW	11/29/2011	COMPAL	EMI final solution for HDMI.	1.L19/L20/L21/L22 de-populated & R459/R451/R462/R466/R468/R469/R470/R471 populated 0 ohm. 2.Change R467 from 499ohms to 510ohms to adjust sigal swing. 3. Pop R486 & R487 to enable HDMI repeater pre-emphasis. De-pop LC filter at HDMI conn. side.	X02
61	17,35,39.	HW	12/05/2011	COMPAL	EMI solution for E-Docking USB port.	Swap USB Port6 and Port8 and reserve a choke at E-Docking conn. side: Port6 from Mini3 Pink Panther card to E-docking Port8 from E-Docking to Mini3 Pink Panther card	X02
62	36	HW	12/05/2011	COMPAL	From ESD team request	Add 0.1u CAP for EXP PWR SW signals, CPUSB#, EXPRCRD_CPPE# and CARD_RESET#	X02

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
63	40,45	HW	12/05/2011	COMPAL	Power over rating when using 65W adapter	Add EC5048 GPIOA7, GPU_PWR_LEVEL to slow down GPU when GPU keeps at high performance mode but using 65W adapter	X02
64	14~21	HW	12/05/2011	COMPAL	Change PCH to C1 (QS) version.	Change UH4 to SA00005BU1L.	X02
65	32	HW	12/06/2011	COMPAL	EMI request for ISN Issue.	Add ESD diode on GND_CHASSIS trace if EMI change C485:1000P to 120P.	X02
66	7	HW	12/06/2011	COMPAL	ESD Request.	RC19.2 change to XDP_DBRESET#_R. RC29.2 change to XDP_TDI_R. RC35.2 change to XDP_TDO_R.	X02
67	24	HW	12/06/2011	COMPAL	EMI request for USBP12.[BITS:DF524330]	Pop L12 and De-pop R427,R428.	X02
68	41	HW	02/01/2012	COMPAL	Change board ID to A00.	Change R875 to 33Kohms.	A00
69	32	HW	02/01/2012	COMPAL	30MHz~50MHz LAN broadband noise.	Modify C485 from 10pF to 150pF.	A00
70	44	HW	02/20/2012	COMPAL	ME Request.	SW1 change to SN11100580L.	A00
71	All	HW	02/20/2012	COMPAL	For cost saving.	Change 0 ohm resistor to short pad, total 14 pcs.	A00
72	28	HW	02/20/2012	COMPAL	For cost saving.	HDD PWR De-pop :R1624, R500, R499, R504,R516,Q28, C393, C394.	A00
73	14	HW	02/20/2012	COMPAL	For cost saving.	De-pop RH288,RH48,RH49,RH47.	A00
74	7	HW	02/20/2012	COMPAL	ESD Request.	De-pop RC30, RC31, RC33, RC34, RC36, RC37, RC38, RC39 .	A00
75	37	HW	02/20/2012	COMPAL	System will reconnect USB 3.0 after resume from S3 issue.[BITS:DF537410].	JBTB1 Pin 38 reserve R154 to +3.3V_ALW_PCH.	A00
76	35	HW	02/20/2012	COMPAL	E4 no support WWAN SMBUS function .	Not stuff R1157 and R1158.	A00
77	36	HW	02/21/2012	COMPAL	Fix EMI issue.	Stuff CE16,CE17 & CE18.	A00
78	37	HW	02/21/2012	COMPAL	Dell E4 NB USB1457 Sansung i9100 S0 issue.	Add Q126 and remove R1613.	A00

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1	55	+1.5V_MEN	7/5	Dell	Follow VC , enable use SIO_SLP_S4#.	Add PR210 for net "SIO_SLP_S4#"	X01
2	53	DCIN	8/4	Dell	ME design change.	PJPDC1 change from 7pin to 5pin	X01
3	54	+5V/3.3V	8/4	Dell	Main and 2nd IC common setting.	De-pop PD100,PR113,PR111	X01
4	60,62 54	Vcore, Charger +5V/3.3V	8/4	Compal	EMI solution.	Pop PL700.PL1300,PL100	X01
5	54	+5V/3.3V	8/4	Compal	DFX concern, choke change from 10*10 to 7*7	PL101 change from 3.3u 10*10 to 2.2u 7*7 PL102 change from 3.3u 10*10 to 3.3u 7*7	X01
6	54 55	+5V/3.3V +1.5V_MEN	8/4	Compal	COS concern, change from D2 Polymer cap to OScon cap	PC110 change from 220u polymer cap to 220u OScon cap PC208 change from 330u polymer cap to 390u OScon cap	X01
7	54 55	+5V/3.3V +1.5V_MEN	8/4	Compal	Prevent Jitter issue.	Add PC120,PC121,PC215 parallel with PR101,PR102,PR207	X01
8	60	Vcore/GFX core	8/4	Compal	Prevent output voltage glitch when power up.	PU700, VCCP and VDD change form +5V_RUN to +5V_ALW	X01
9	64	GPUcore	8/4	Compal	Prevent output voltage glitch when power up.	PU1000 VCCP and VDD change form +5V_RUN to +5V_ALW	X01
10	60	Vcore/GFX core	8/4	Compal	DFX concern.	Change PU701,PU702 from ISL6208(3x3) to ISL6208B(2x2).	X01
11	60	Vcore/GFX core	8/4	Compal	Fine tune the VCORE and VGFX Load Line	Change PR749 from 3.57K to 3.48K Change PR702 from 3.57K to 4.64K	X01
12	60	Vcore/GFX core	8/4	Compal	Fine tune the VCORE and VGFX transient response	Change PC733 &PC705 from 47pF to 68pF Add PC702 0.022uF	X01
13	62	Charger	8/4	Compal	Change the component to HF parts	Change PQ1306 & PQ1308 from SB50206008L to SB57002040L	X01
14	53	DCIN	10/17	Compal	Reduce power consumption in S5.	Add PCH_ALW_ON for +PWR_SRC_S enable signal.	X02
15	64	GPUcore	10/17	nVidia	Deep sleep mode control.	Add DPRSLPVR_R signal connect to GPU.	X02
16	60	Vcore/GFX core	10/17	Compal	Fine tune the VCORE transient response	Add PC747 68nF	X02

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1	54-64		10/20	Compal	For cost saving, change the 0ohm resistors to layout short PAD.	Footprint change PR100,PR116,PR208,0R210, PR306,PR403,PR503,PR508,PR513,PR600,PR602, PR604,PR607,PR612,PR716,PR730,PR732,PR735, PR1300,PR1302,PR1312,PR1320,PR1339,PR1342, PR911,PR925,PR937,PR941,PR932,PR936,PR926, PR935,PR945,PR947,PR949,PR939,PR940,PR943, PR948,PR951,PR955,PR957,PR961,PR953,PR954, PR956,PR958,PR959,PR960,PR963,PR1005,PR1006, PR1011,PR1014,PR1016,PR1018,PR1017,PR1026, PR1029	X02
2	55	+1.5V_SUS	10/20	Compal	Fine tune OCP.	PR201 change form 5.1K to 6.34K.	X02
3	57	+1.05VM	10/20	Compal	Fine tune OCP.	PR402 change form 60.4K to 110K.	X02
4	58	+1.05VTT	10/20	Compal	Fine tune OCP.	PR501 change form 84.5K to 110K.	X02